Design a Low Noise Amplifier at 25.8 GHz for 5G Millimeter-Wave at Vietnam and Other K/Ka Band Applications using MMIC Technology

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***Abstract*— In this paper, we propose a design diagram of low noise amplifier using NP2500MS transistor 0.25 µm AlGaN/ GaN HEMT technology of WIN Semiconductor, Taiwan, consisting of 2 stages at center frequency 25.8 GHz, this is the frequency band used for 5th Generation Mobile Communications of Vietnam and some other K/Ka-band applications. With this transistor, the LNA has achieved a noise figure less than 1.62 dB and and Gain average is 13.1 dB in the whole bandwidth.**

Keywords*— *LNA for 5G Millimeter-Wave, LNA Ka two stages.

I. INTRODUCTION

Low Noise Amplifier (LNA) is very important role in the receiver input front of the radio communication systems, they are an important part in improving the sensitivity and reducing the noise of the whole of radio receiver. They amplify the input signal with a minimal amount of noise before the signal is processed in the following stages of the receiver. Therefore, good LNA design should be well thought out and based on numerical values such as low noise, average gain, linearity and stability. Nowadays, some applications such as those related to radio astronomy, satellite communications or next-generation mobile communications in the Ka-band are often required to have LNAs with very low noise throughout the working frequency range. MMIC (Monolithic Integrated Circuit) technology is the key to the design of LNA circuits at ultra-high frequency with low noise factor, compact size with high gain and reliability.

In Vietnam, the 5th generation mobile communication uses the end of the K band and the beginning of the Ka band with frequencies from 24.25 GHz to 27.5 GHz. In this article, the author proposes how to design a LNA with a bandwidth of more than 3.25 GHz that can be used for 5G mobile communications at the center frequency of 25.8 GHz using a GaN material FET transistor with high electrical mobility. High Electron Mobility Transistor (HEMT), the design process is done on Keysight ADS software with MMIC models and components provided by the company. The design objectives and parameters are presented in Table 1. The complete design of the 2-stage amplifier along with the design approach, design objectives and simulation results will be presented in the following sections with brief discussion.

TABLE 1: DESIGN GOALS OF THE LNA

Frequency (GHz)	25.8
Noise Figure (dB)	<1.7
Gain (dB)	>12
3dB Bandwidth (GHz)	>3.5
Input Return Loss (dB)	>4
Output Return Loss (dB)	>20
P1dB (dBm)	>18

II. CIRCUIT DESIGN

For this LNA MMIC design, the author uses a 125 µm gate-width (UGW) transistor of HEMT technology on a 100 µm-thick GaN platform from WIN SEMICONDUCTOR company, Taiwan. All models, process design kits (PDKs) are provided by the manufacturer. This transistor can operate up to 50 GHz which is completely satisfactory for design with our goal of achieving low noise figure, high gain, small output return loss and compact size. Besides, the bandwidth is required more than 3.5 GHz [3].

In Figure 1, we propose the principle diagram of the LNA set of 2 stages [1]. The first stage is designed to optimize the noise figure with a wide-band input circuit. The second stage is designed to give priority to the amplification and the impedance matching between the two stages is designed in order to broadband too and convenient to supply DC power. The output impedance matching circuit also uses broadband matching. All the impedance matching circuits use terminal open-circuit high impedance transmission lines with optimized dimensions, they help thel size of the circuit after layout not too large.

In order to reduce the noise figure, determining the working point for each transistor is very important, the first stage is designed with the goal of small noise, minimum DC power but still to establish the transistor's working mode in the positive region with stable unconditionally and the smallest possible power consumption. Details, the supply voltage for the Drain pole of the first transistor is selected V_{DS1}=10 V which is the minimum value for the transistor to operate in the possible region, the supply voltage for the Gate pole is selected V_{GS1} =-2.4 V, I_{D1} = 38 mA , with this working point, the lowest noise figure of this stage can reach NF_1=0.82 dB in theory. The second stage is designed with the goal large gain while the noise figure is not too large. The DC parameters of the second stage are V_{DS2} = 10.5 V, V_{GS2} = -2.2 V, I_{D2} = 53 mA. With this selection, the minimum noise figure of this stage NF_2 = 1.24 dB while the gain can reach more than 8 dB. Powering for transistors is through inductors L_1, L_2, L_3, L_4 combined with a high impedance transmission line (TL) [2] to ensure that at the design frequency 25.8 GHz they have a very large impedance compared to the impedance of transmission line.

Figure 2 descripte the LNA after layout, all elements used for the design are MMIC components provided by the manufacturer including inductors and capacitors, all integrated on a monolithic chip. The size of the whole circuit after lay out is achieved at 3.7mmx1.6mm. This is a not too large size for an amplifier circuit operating in this frequency range.

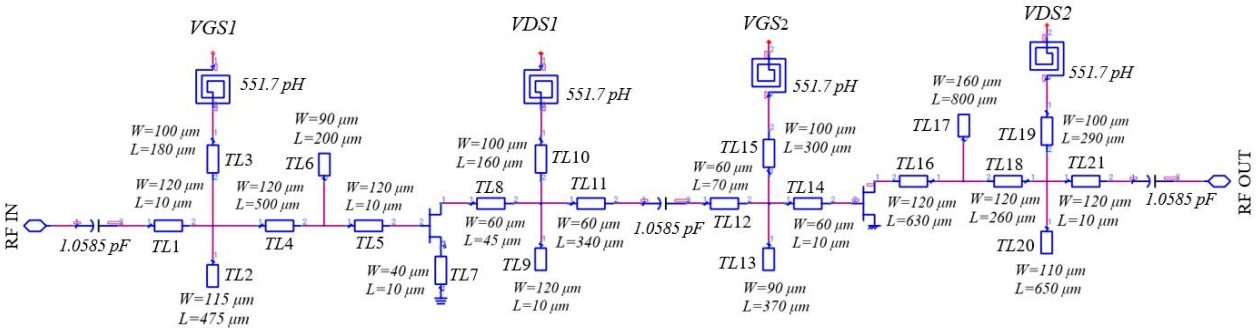

Figure 1. Schematic Diagram of Proposed LNA MMIC

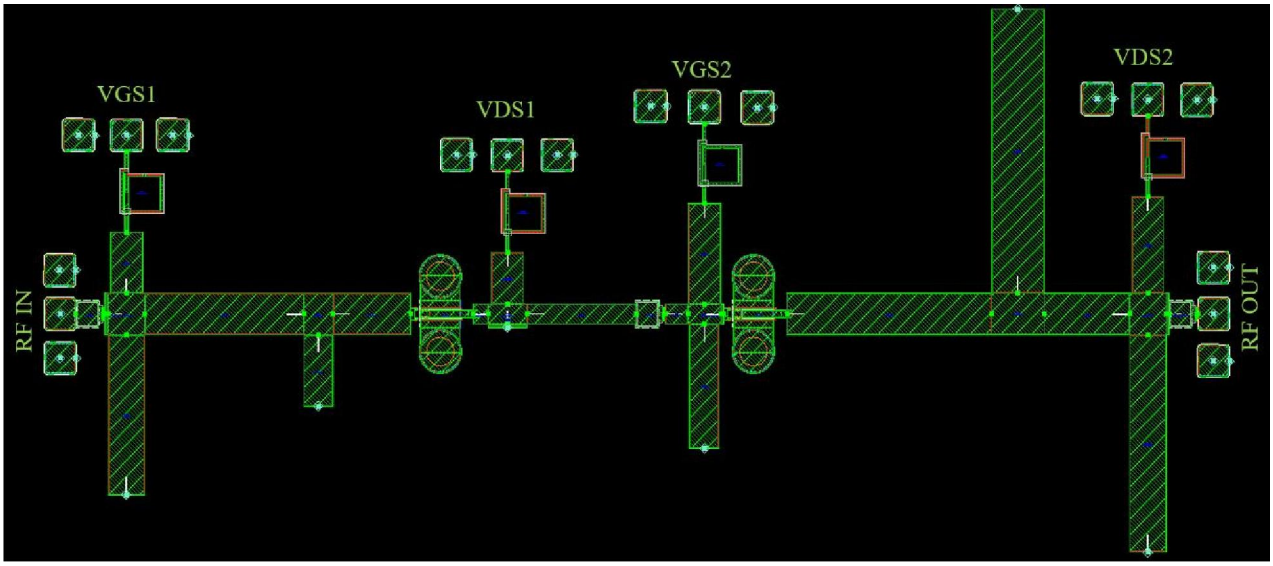

Figure 2. LNA MMIC Layout

III. SIMULATION RESULTS

Figure 3 shows the simulation results of the gain and noise figure of the designed LNA:

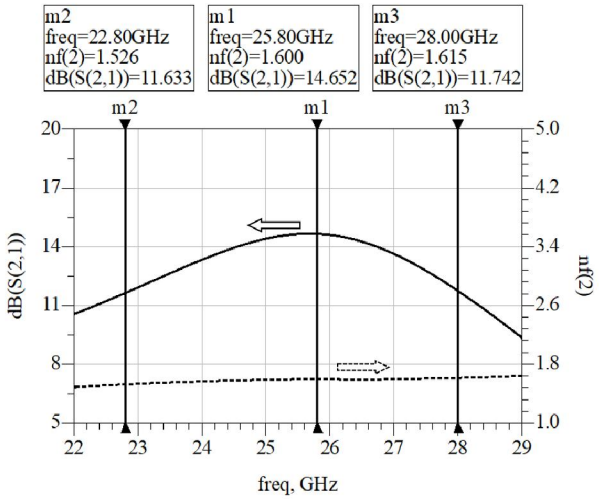

Figure 3. Gain and Noise Figure

We can be see that at the center frequency the gain is 14.65 dB while the noise figure at the center frequency is 1.6 and in the bandwidth (from 22.8 GHz to 28 GHz), it fluctuates small from 1.58 to 1.62. In addition, we also see that the the bandwidth of the LNA is quite wide, up to 5.2 GHz, thus covering the mobile 5G band in Vietnam.

Figure 4 shows the I/O return loss and isolation of the LNA, it can be seen that the output impedance matching is quite good while the input must sacrifice coordination to achieve the low noise figure. The best S22 is -29.4 dB at center frequency while the S11 is -5.1 dB , the isolation factor in the whole bandpass is better than -50 dB. This result shows that the design method is suitable in this condition using this transistor because for LNA, the input signal is very small, so it is acceptable for S11 to be quite large to achieve good noise figure. At the output, when the signal is amplified, if S22 is not good, it will damage the amplifier circuit. Therefore, the author gives priority to low noise, gain is moderate because LNA is the first stage of the receiver, low gain can be compensated by intermediate amplifier stages of the receiver.

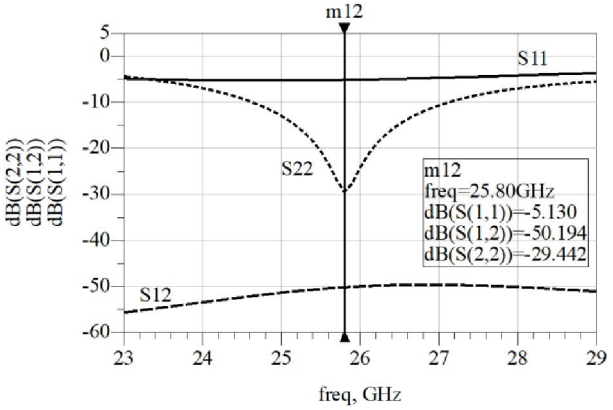

Figure 4. I/O return loss and isolation

Figure 5 describes the simulation results of large signal level of the LNA circuit. We see that at the P1dB, the Gain is achieved by 13.6 dB while the output power is 18.8 dBm.

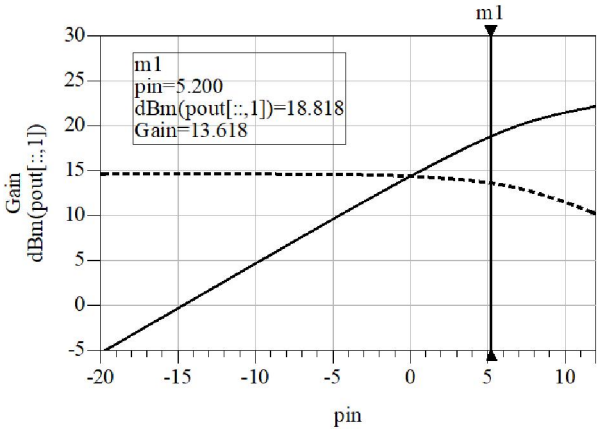

Figure 5. P1dB (dBm)

Figure 6 shows the stability factor (K) of the LNA from 22 to 29 GHz. It is clear that K>18 in the entire frequency range ensures the unconditional stability of the LNA MMIC.

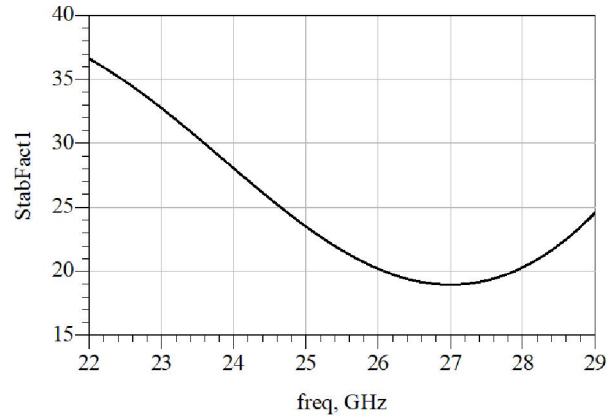

Figure 6. Stability Factor

The results of this design at center frequency 25.8 GHz are showed in Table 2. Clearly, the results obtained of this design satisfy the stated requirements. This is a pretty good result when comparing the proposed design with other works listed in Table 3.

TABLE 2. ACHIEVED RESULT

Parameters Stability	Design Requirements	Achieved Results
Noise Figure (dB)	< 1.7	<1.62
Gain (dB)	>12	14.6
Input Return Loss (dB)	>4	5.1
Output Return Loss (dB)	>20	29.4
3dB Bandwidth (GHz)	>3.55	5.2
P1dB (dBm)	>18	18.8

Particulary, comparing with some articles and other works with 2-stage diagrams in Table 3 using CMOS and GaN technology with little different diagrams, we can see that the proposed design has noise figure significantly lower (<1.62 dB in the bandwidth) while all other works give noise greater than 3 dB. Regarding the gain, we can see that the gain of the proposed design is approximately [8] using 0.12-µm InAlGaN/GaN HEMT, which is higher than that of [4], [7] using 130 nm CMOS and 0.2-µm GaN HEMT and lower [5], [6] using CMOS with configuration differential two-stage diagram. In terms of bandwidth, the proposed design is still quite outstanding with [4], [5] và [6] when it has a fairly wide bandwidth (5.2 GHz) to meet the requirements of many systems. Regarding the I/O return loss, we can see that the input loss is highter compared to all other designs but the output loss is good. This has been explained above, this result is completely consistent with the working conditions of the LNA when working with very small input signals, so the return input loss of 5.1 dB is the acceptable result. Regarding DC power consumption, clearly CMOS technology is an advantage, better than GaN HEMT, because of the large DC power consumption (large V_{DS} and large I_D) so the P1dB of GaN is higher than CMOS technology. In fact, depending on the requirements of the circuit, we can choose the suitable design.

Concluding the discussion on comparing the results of Table 3, we see that each scheme and technology has its own advantages and disadvantages, however, our idea is that although the Differential circuit structure gives a higher efficiency in terms of gain, but it uses a larger number of transistors and the structure of LNA circuit would be more complicated, this would cause high noise and that would be completely unsuitable for MMIC design because with monolithic integration, all active and passive components are components. integrated into the monolithic circuit and provided by the manufacturer, there are not many options for passive elements such as L and C, so the complex circuit structure will bring many difficulties in the design process, adjust the impedance matching circuit as well as optimize the size, simulation, measure and evaluate the results, that's the reason why the author's design direction select the simple design, easy to implement, suitable for MMIC design that brings good effect, focusing on reducing the noise, bandwidth expansion, good output return loss and gain is moderate, because gain can be compensated by the following amplification stages of the receiver.

TABLE 3. COMPARISONS OF MILLIMETER LNA WITH CMOS TECHNOLOGY

Parameter	**[4]**	**[5]**	**[6]**	**[7]**	**[8]**	**This work**
Frequency (GHz)	24	24	23.5	1-25	33-41	25.8
Topology	2-stage Single	2-stage Differential	2-stage Differential	2-stage Feedback	2-stage Single	2-stage Single
Noise Figure (dB)	<3.7	<4.7	<3.6	<3.1	<4	<1.62
Gain (dB)	<9.2	<19.8	<20	<13	<15	<14.6
Tech	130 nm CMOS	180 nn CMOS	90 nm CMOS	0.2 µm GaN HEMT	0.12 µm InAlGaN/GaN HEMT	0.25 µm AlGaN/ GaN HEMT
3dB Bandwidth (GHz)	3.7	4	2	N/A	N/A	5.2
Input return loss (dB)	12	N/A	16	14	13	5
Output return loss (dB)	16	N/A	24	32	16	29
P1dB (dBm)	-13	-12	N/A	17.5	13	18.8
Pdc (mW)	2.78	48	16.5	1000	280	937

IV. CONCLUSTION

In summary, the design results were satisfactory compared with the technical criteria set out in Table 1. The content of the article presented an optimized LNA with 2 amplifier stages using MMIC technology with bandwidth from 22.8 GHz to 28 GHz that can be applied for 5th generation mobile communication and other radio applications at Ka band in Vietnam. This is also a good choice with design requirements with low noise factor, small output return loss and medium gain. The comparison results with some articles using CMOS and same technology, we can see advantages and disadvantages of each technology and each diagram with the highlight is the low noise figure belong to GaN HEMT technology. These show the suitability of MMIC for high-bandwidth applications at K, Ka band and higher bands with growing applications such as satellite communication, radar, mobile, astronomy. The article is also a basis to optimize the design for many representative stages in LNA circuit and RF circuit for designer can refer and compare.

ACKNOWLEDGMENT

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