Flexible and low-cost FPGA-based MCA for development of handheld measurement devices

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Abstract

This paper presents a full procedure for developing a flexible and low-cost field-programmable gate array (FPGA)-based multichannel analyzer (MCA). Digital signal processing (DSP) algorithms, including a digital Sallen-Key filter, energy reconstruction (trapezoidal) filter, baseline restorer, timing trigger, and pulse pile-up rejector, are implemented on FPGA. Without using an analogue signal conditioning circuit, this digital MCA is coupled directly to the detector pre-amplifier, leading to a simple, compact, and cost-effective hardware design. All filter parameters have been optimized via simulation in MATLAB/Simulink with digitized pulse data from a high-speed analog-to-digital converter (ADC). A temperature stabilization algorithm has also been integrated in to the FPGA as a digital gain compensation module. Custom software for acquisition and analysis with a user-friendly graphical interface is used to control this MCA. This prototype system is highly promising for the development of handheld radiation measurement devices in terms of performance, cost, and size.

Keywords: Digital signal processing (DSP), field-programmable gate arrays (FPGAs), multi-channel analyzer, filter, algorithm.

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1. Introduction

Traditional analogue spectroscopy systems consist of a charge-sensitive preamplifier (CSP), pulse shaping amplifier, analog-to-digital converter (ADC), and multichannel analyzer. However, analogue electronic components are susceptible to noise, consume a lot of power, and provide a limited filtering. Analogue filters typically apply a combination of differentiations and integrations of the voltage signal to transform it into a Gaussian-like shape, and several filters is previously impossible to implement on the traditional analogue pulse processing system. High-performance intergrated circuits (ICs), such as field-programmable gate arrays (FPGAs) and flash ADCs, have overcome these limitations. In addition, digital multichannel analyzers (DMCAs) combining FPGAs and high-speed ADCs have been developed [1, 2, 3, 4, 5, 6]. Due to their advantages, including compactness, low cost, low noise, thermal stabilization, and low power consumption, these systems are commonly used in nuclear instruments. The incredible performances of these systems are achieved via their recursive mathematical algorithms in addition to their signal processing hardware systems. For instance, a compact and low-cost DMCA with a multi-input channel was introduced in [3]. However, this DMCA is based on a large ARM/FPGA development board and featuring peripheral elements that are not necessary for nuclear signal processing, making it impossible to use on a small handheld device. In addition, the LabVIEW platform was used to build the acquisition and analysis software in this system and some of the others was also built as a Visual Instrument [1, 2, 3]. This platform can capture, and validate signals, take measurements, and visualize data with less effort than traditional programming environments; however, creating a modern customized user interface can be challenging in LabVIEW. The authors of [5] investigated adaptive digital pulse shaping in a reconfigurable FPGA using the LabVIEW FPGA Module. According to experimental testing, higher throughput can be achieved while maintaining the energy resolution observed utilizing longer shaping time. A National Instrument 5761 14 bit, 250 MS/s adaptor was used for digitizing the exponential decay pulses in the above-mentioned system. This module was designed to work in conjunction with the NI FlexRIO™ FPGA module[7], resulting in a high performance but costly measurement system. Furthermore, none of the DMCAs that have been developed connect to, and process data from a temperature sensor [1, 2, 3, 4, 5, 6]. The ambient temperature value is a critical parameter in environmental monitoring and stabilizing the measured gamma spectra, especially in a system using scintillation detectors. Low-cost, multi-channel analyzer systems for γ-ray spectroscopy featuring PC sound cards were introduced by authors of [8, 9]. Signal conditioning unit were used in these systems, which included CR-RC^n shaping circuits, as well as various pole-zero cancellation and base line restorer options. The authors of [10] recently proposed a zero-cost DMCA system based on digital signal processing (DSP) technology, in which digitized data is processed on a personal computer using recursive algorithms. This system also used a PC sound card for data acquisition. However, the low sampling rates of the built-in ADCs in PC sound cards (48-192 kHz) limit the use of the last three systems in nuclear physics laboratory teaching applications. Currently, several DMCAs are available as commercial systems [11, 12], but they are expensive and inflexible, as the users cannot reconfigure the FPGAs. In contrast to these commercial systems, an FPGA-based MCA for spectroscopy has many advantages. The most valuable feature of such a system is its flexibility, i.e., it can be adjusted for different applications by via modification of the FPGA's programming.

This paper presents a flexible and low-cost FPGA-based MCA for environmental measurement application featuring a stand-alone board. A custom-made printed circuit board (PCB) was designed to reduce the size of the board, remove unnecessary peripherals, and optimize power consumption. In addition, acquisition and analysis software was developed to control this DMCA and provide a real-time option for spectrum analysis. Our prototype DMCA was tested with a 3"×3" NaI(Tl) scintillation detector with different radiation sources. The results were then compared to spectra measured with a commercial DMCA. Furthermore, an advanced algorithm for temperature stabilization was successfully implemented in the FPGA, allowing the DMCA to minimize the effect of temperature variation on the measured gamma spectra in real-time. The prototype system is highly promising for the development of handheld radiation measurement devices in terms of performance, cost, and size.

2. Material and methods

2.1. Hardware description

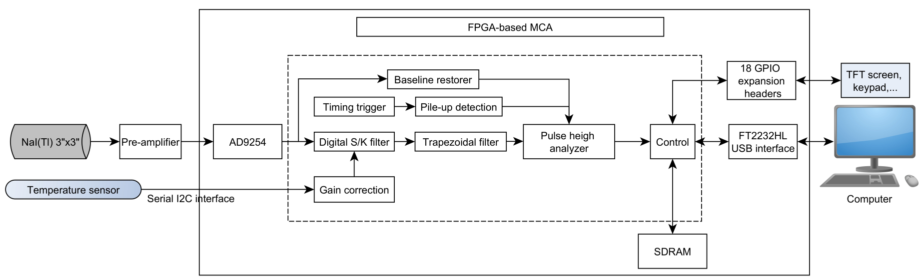

Figure 1: Block diagram of the prototype DMCA

Fig.1 illustrates the block diagram of the developed DMCA. The system was developed using an FPGA (model MAX10 10M50SAE144I7G, Intel Corp., USA[13]) and a high-speed 14-bit ADC (model AD9254, Analog Devices, USA[14]) with a sampling rate of up to 150 MSPS (mega samples per second). The utilized FPGA has 50,000 logic elements, an industrial operating temperature range (-40℃ to 100℃) and can reduce its power usage 95% in sleep mode. Featuring a high-speed sampling rate and flexible analogue voltage input range, combined with power and cost savings over previously available ADCs, the AD9254 is suitable for communications, medical ultrasound, and spectrometer application, particularly when considering its power and cost savings over previous available ADCs. A 265MB SDRAM (model AS4C16M16SA, Alliance Memory, Inc., USA [15]) is utilized to store measured spectra. Communications between the DMCA and computer are carried out via an IC with a USB controller (model FT2232HL, FTDI Chip, USA[16]). The FT2232HL is a dual high-speed USB to multi-purpose UART/FIFO IC with a data transfer rate of up to 480 Mbits/second. The block diagram of the DMCA is shown in Fig.1. The 100 MHz clock rate synchronizes both the FPGA and the flash ADC. The entire system is powered by a 5.0 VDC power supply and the overall power consumption is around 1.5W. To minimize the electrical noise, PCB size, and power consumption, no analogue signal conditioning circuit is used suggested system design.

The characteristic of the proposed DMCA and recent studies are summarized in Table 1.

Table 1 demonstrates that the proposed design of the DMCA covers advanced features in comparison with recent studies including high-speed ADC, high data communication speed, compact, and low-cost.

2.2. Digital signal processing

The output signal from the pre-amplifier is directly digitized by the flash ADC. Then the output code of ADC is captured and synchronized to the FPGA by the data clock output (DCO) signal. The AD9254 provides a DCO signal intended to capture the data in an external register. The digitized signal is passed through the Sallen-Key (S/K) digital filter to remove high-frequency components [17]. The recursive model of the digital S/K filter is described in (1) below:

$$y_n = \frac{\left(k.\left(3-a\right)+2.k^2\right).y_{n-1}-k^2.y_{n-2}+a.x_n}{1+k.\left(3-a\right)+k^2} \tag{1}$$

where $k = \tau/\Delta t$, with τ representing the time constant of the S/K filter, and Δt indicating ADC sampling interval, and a represents the gain coefficient. The digital S/K filter was simulated in MATLAB/Simulink to find the optimal cut-off value in the frequency domain. The actual input signal from the pre-amplifier and corresponding output signal at different values of a and k are shown in Fig.2.

Table 1: DMCA architecture in comparison in recent studies

	This work	DMCA in [1]	DMCA in [2]	DMCA in [3]	DMCA in [4]	DMCA in [5]	DMCA in [6]
FPGA chip	Intel MAX10	Xilinx Spartan2	STM32F407	Zynq – 7000	Xilinx Spartan3	Kintex-7	Intel Cyclone III
ADC chip	AD9254	Not specific	ADS807	AD7476	AD6645	NI 5761	AD9265
ADC resolution	14-bit	12-bit	12-bit	12-bit	14-bit	14-bit	16-bit
ADC sampling rate	100 MSPS	40 MSPS	42 MSPS	1 MSPS	62.5 MSPS	250 MSPS	100 MSPS
RAM	256 MB SDRAM	Build-in RAM	Not specific	Build-in RAM	Build-in RAM	2 GB DRAM	Not specific
Data communication interface	High-speed USB interface	Serial RS-232	High-speed USB interface	High-speed USB interface	Serial RS-232	Not specific	High-speed USB or RS-232
Cost estimation	$300	Not specific	Not specific	$479	Not specific	$22,362	Not specific

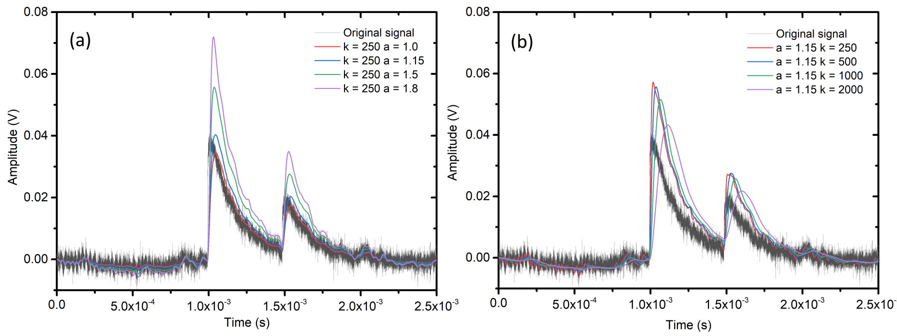

Figure 2: Input and output signals from the digital Sallen-Key filter

The shape of the output signal is strongly influenced by the coefficients a and k. As can be seen from Fig.2a, a larger a value results in a higher output pulse amplitude. On the other hand, as shown in Fig.2b, a larger k value will lengthen the rising edge of the input pulse, increase the pulse width, and decrease the pulse amplitude. In this study, a and k were chosen as 1.15 and 250, respectively, resulting in a cut-off frequency of 30 kHz.

One of the most important factors affecting the quality of a digital gamma spectrometer is the algorithm that converts any exponential pulse with a large decay time constant from the CSP to a suitable form to extract the amplitude and reduce the pulse pile-up phenomena. Several DSP algorithms were considered for the DMCA's digital pulse shaping, including trapezoidal, Gaussian, cups-like filter [18], moving window deconvolution [19], Fourier transform [20], and Mexican hat wavelet pulse [21]. Due to their outstanding characteristics, such as the best signal-to-noise ratios, and ballistic deficit reduction [18], trapezoidal pulse filters are widely used in digital pulse processing systems for nuclear equipment. In this study, a trapezoidal pulse filter is utilized as an energy reconstruction filter. The theorem describing, and simulation of, a trapezoidal filter are described in [22], both based on the following transfer function in the z-transform domain (2):

$$F_{trapezoidal}(z) = (1-\beta z^{-1})\left(\frac{1-z^{-R}}{1-z^{-1}}\right)\left(\frac{1-z^{-(R+M)}}{1-z^{-1}}\right)\left(\frac{z^{-1}}{R}\right) \tag{2}$$

where $\beta = e^{\frac{-\Delta t}{\tau_{preamp}}}$ is the pole-zero coefficient, with Δt indicating the sample interval of the flash ADC, and τ_{preamp} representing the decay time constant of the CSP, and R and M are the duration of the rising edge and flat-top of the trapezoidal pulse, respectively.

The timing trigger generator, pulse baseline restorer, pile-up rejector, interface controller, and computer communications are controlled by the FPGA. The timing trigger generator transforms the exponential input signal into an appropriate signal shape to obtain the timing information of the pulse, thereby generating the control signal for extracting the pulse amplitude, base line determination, and pile-up inspection. The transfer function for the timing trigger generation in the z-transform domain, also called the CR-RC^2 filter, is described as follows:

$$F_{timingtrigger}(z) = \frac{z^{-1}(1-z^{-S})}{1-z^{-1}}(1-z^{-D})(1-z^{-D}) \tag{3}$$

where S is window point in the moving average filter, and D is the differentiation parameter. Usually, the value of D is chosen to be equivalent to the rise time of the signal from the pre-amplifier. The timing trigger generator converts an exponential pulse to a bipolar pulse with the a zero crossing time that does not depend on the pulse amplitude (similar to the Constant Fraction Discriminator module in a conventional analogue system). Before being transferred to the histogram memory, the amplitude extracted from the trapezoidal filter is subtracted from the baseline value, which is derived from the baseline restorer module by averaging the input signal value when the radiation pulse nor present. The average number of baseline determinations is set to 16 for a low input count rate and 8 for a high input count rate in order to reduce the system's total dead time. The pulse pile-up detection is inspected at the end of the trapezoidal flat-top. The extracted pulse amplitude is considered valid if no signal from the timing trigger generator for another pulse occurs during this inspection. The timing diagram of these DSP modules is presented in Fig.3.

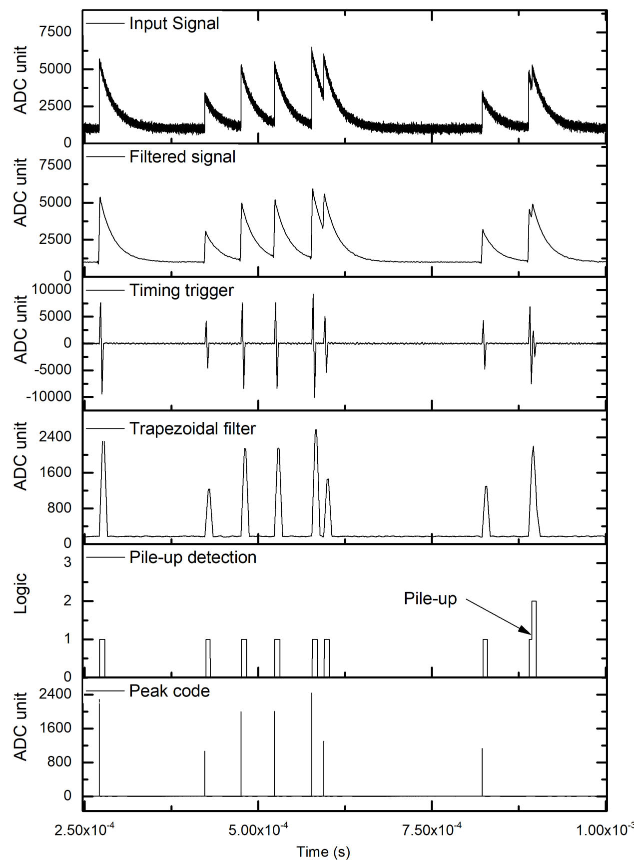

Figure 3: Timing diagram of the DSP modules implemented in FPGA

The gamma spectrum obtained via a scintillation detector for long-time measurement with an in-situ temperature is unstable, leading to photopeak shifting and spectrum distortion [23]. Recently, we proposed an advanced method for stabilizing the gamma spectra based on experimental data recorded under the controlled temperature conditions in the laboratory [24]. However, the stabilization algorithm was performed by the central control software with a correction interval of 10 minutes. In this study, we chose to implement the proposed algorithm in the FPGA as a digital gain compensation module. The temperature value is taken directly from an external temperature sensor (Model SHT30-SJ57, Sensirion Company, Switzerland [25]), and the pulse amplitude is corrected every 30 seconds during measurements. The histogram data is stored in the internal memory and then transferred to the PC using an FT245 Style Synchronous FIFO Interface with 40 MB/s data transfer rate. The transmission interval is set to 1 second by default and can be reconfigured.

2.3. Acquisition and analysis software for the DMCA

A few previous studies have developed DMCA user interfaces, but most of the software was designed on the LabVIEW platform to act as virtual instruments (VIs) [2, 3]. In this study, a custom-made acquisition and analysis software is used for this prototype DMCA that features a friendly graphic user interface (GUI). This application uses the C# language and D2XX library [26] to ensure high-speed communication with the DMCA. The analysis modules includes peak searching, peak fitting, energy and efficiency calibration, and nuclide identification. Fig.4 shows the visual GUI of the application. The control buttons are located right on the main screen, and the observed count rate indicator, timing information, and measurement mode are displayed. The left side of the screen shows the real-time measured spectra on a linear or logarithmic scale.

2.4. Performance evaluation of the DMCA

Several benchmark tests with commercial PMT-based 3"×3" NaI(Tl) (model 12S12/3.VD.PA.HVG, ScintiTech Inc., USA [27]) using ^{137}Cs and ^{60}Co calibration sources are carried out. The prototype DMCA performance is compared with a commercial DMCA APG7300A (TechnoAP, Inc., Japan [11]). The radiation sources with different activity and source-to-detector distance are also varied to achieve input count rates from approximately from 1 kcps to 165 kcps. Because the APG7300A commercial DMCA processes Gaussian pulses only, the signal from the pre-amplifier is passed through a CANBERRA Model 2022 Spectroscopy Amplifier (2022 S.A.) before being fed to this DMCA. The

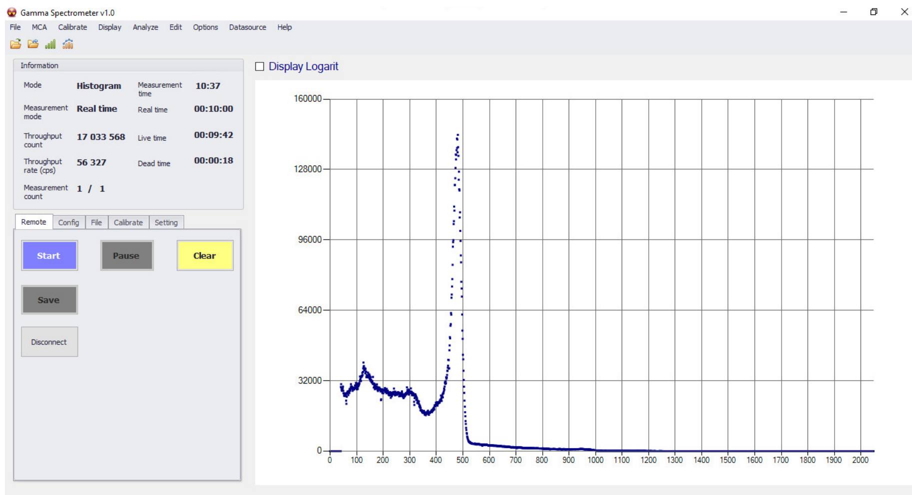

Figure 4: The software's graphic user interface

signal from the CSP is transferred simultaneously to the prototype DMCA and 2022 S.A. via a signal splitter module, namely, an MT050 (ORTEC[28]). The shaping time for the 2022 S.A is set at 1μs, and the peak detect configuration of the APG7300A MCA is done in "fast mode" with a fixed 250 ns of dead time to obtain a maximum throughput rate. The experimental set-up is shown in Fig.5.

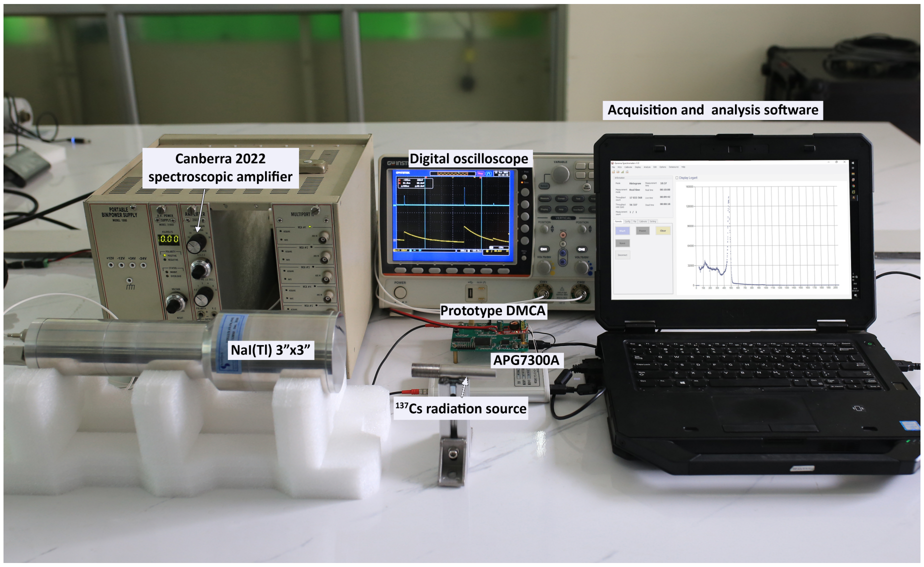

Figure 5: Experimental set-up for benchmarking the prototype DMCA

190 ## 3. Results

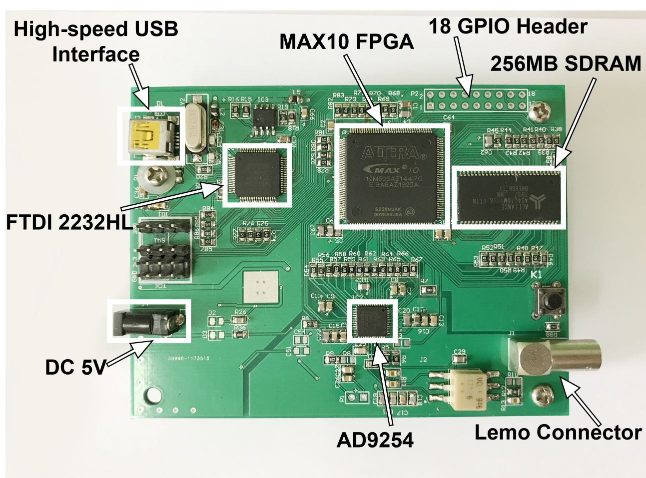

Figure 6: Hardware layout of the prototype DMCA

Fig.6 shows the DMCA's complete hardware design. The key components are arranged on a 75×95 mm^2 PCB and the entire system weighs only 38.8 grams. For DSP implementation, only 5% of the logic elements and 25% of the memory of the MAX10 FPGA are used. This configuration can be extended with two detector inputs for timing, coincidence measurements, and so forth. This DMCA is compatible with several types of detectors with output signals ranging from ±1 Vpp to ±2 Vpp. For communication with external peripherals, such as TFT displays, keyboards, and sensors, an 18 GPIO-pin expand header is made. The DMCA can also communicate with computers or other microcontrollers directly at high speed, and the channel number for the histogram is maintained in a range from 256 to 16k by the control software.

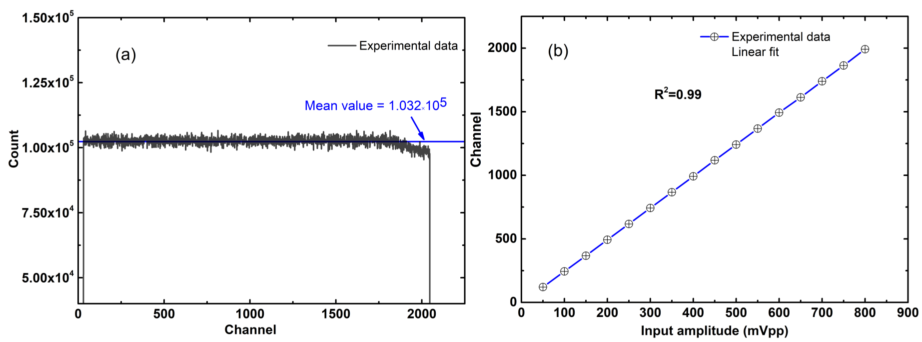

Figure 7: (a) Differential and (b) integral nonlinearity of the DMCA

The integral and differential linearity of the DMCA is tested using the Gwinstek AFG3032 universal pulse generator[29]. Fig.7a and Fig.7b show the differential and integral nonlinearity of the DMCA, respectively. As can be seen, the channel positions have good linearity with the corresponding input signal amplitude. The integral and differential linearity of the DMCA are 0.13% and 1.20%, respectively (in the 90% dynamic range). This linearity is better than those of some previously developed DMCAs [1, 4] and is comparable with some commercial DMCAs [11, 12].

The rise and flat-top times of the trapezoidal shaping filter are optimized for each type of detector via simulation in MATLAB/Simulink. Using the optimal values of the filter parameters, the DMCA developed in this study can effectively suppress the ballistic deficit and extend the throughput. The simulated output pulse shapes, 662 kev photopeak energy resolutions and dead times for different rise time values are presented in Fig.8. In Fig.8a, it can be seen that too short of a rise time in the trapezoidal filter can lead to an incorrect pulse amplitude; for the input signal from the NaI(Tl) detector, this parameter should be chosen as 1÷2 μs to improve the whole system's counting speed while maintaining the energy resolution, as shown in Fig.8b.

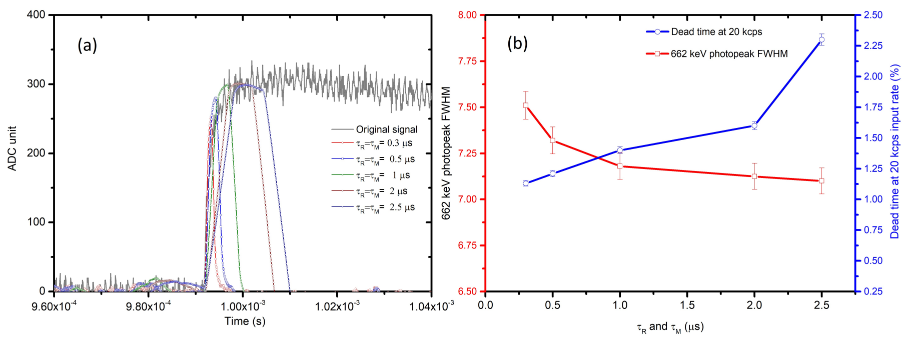

Figure 8: (a) Simulated output pulse shapes, (b) energy resolutions of the 662 keV photopeak, and dead times at an input rate of 20 kcps for various rise times τ_R and flat-top times τ_M for the NaI(Tl) scintillation detector.

Fig.9 shows the throughput rate, dead time, FWHM (Full width at half-maximum) of the 662 keV photopeak, and relative peak position of 662 keV photopeak as functions of the input count rate obtained for our prototype DMCA and APG7300A DMCA. Fig.9a indicates a linear correlation between the throughput rate and the input count rate for up to 50 kcps for both DMCAs. However, at a 100 kcps input count rate, the throughput rate for the APG7300A drops marginally, while the proposed DMCA's linearity remains acceptable. As can be seen in Fig.9b, the dead time of the developed DMCA system is significantly smaller than that of the APG7300A, especially at high counting rates.

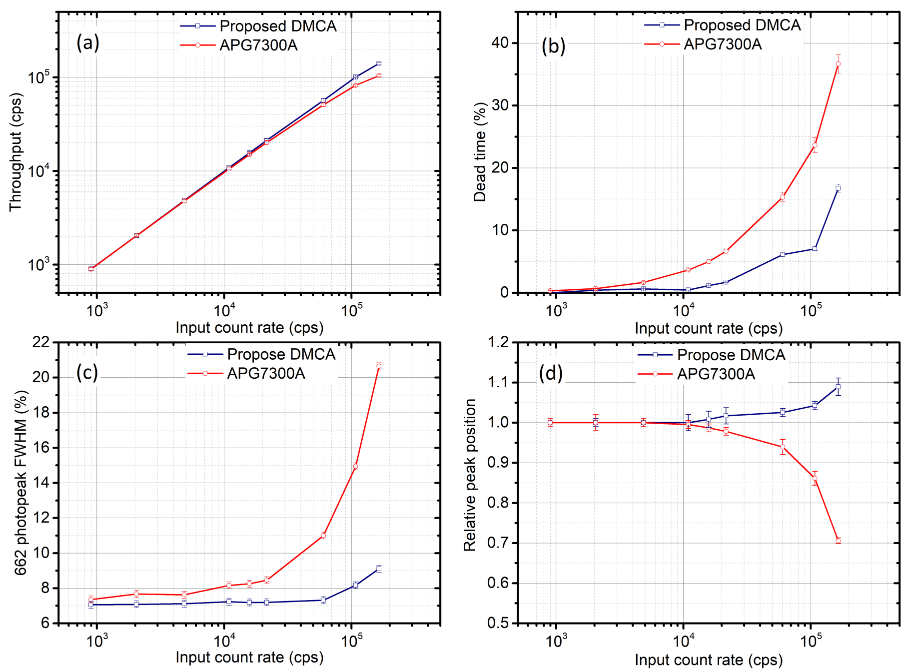

Figure 9: Variations in (a) throughput rate, (b) dead time, (c) FWHM of the 662 keV photopeak, and (d) relative peak position of the 662 keV photopeak for the gamma spectrum measured with ^{137}Cs at different input rates.

The dead time of our proposed DMCA is 7.03% at a input count rate of 100 kcps. The energy resolution and relative peak position of the 662 keV photopeak are dependent on the input count rate for both DMCAs, as shown in Fig.9c and Fig.9d, respectively. With a counting rate of less than 50 kcps, the energy resolution of our DMCA is generally steady. It increases slightly for 50 kcps and above. In contrast, the energy resolution of the APG7300A increases rapidly at a counting rate of 50 kcps or higher. This increase in energy resolution at high count rate is due to the simultaneous peak position shift to the lower region and photopeak distortion.

Fig.10 shows the gamma spectra obtained for our proposed systems and APG7300A DMCA using ^{60}Co radioactive sources at counting rates of 18 kcps

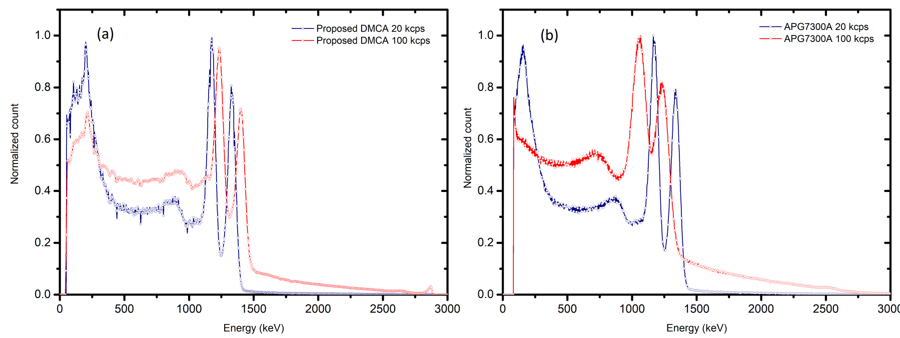

Figure 10: ^{60}Co gamma spectrum obtained for the proposed DMCA and APG7300A DMCA at counting rates of 18 kcps and 100 kcps. The energy calibration is performed 18kcps input count rate

and 100 kcps. The photopeak positions on the spectrum acquired by our system have shifted slightly, as shown in Fig.10a, and the energy resolution of 1332 keV photopeak has increased from 4.83% to 4.92%. Meanwhile, the spectrum obtained with the APG7300A has a stronger shift and energy resolution increases from 5.4% to 7.9%.

The ^{137}Cs 662 keV photopeak locations and the corresponding temperature values are shown in Fig.11. The ambient temperature ranged from 19∘C to 27∘C during the test. In our previous work, our suggested method of stabilization was tested in real scenarios [24], but the algorithm was not yet integrated into the FPGA. However, in this work, the set of temperature correction coefficients has been added to the DSP system as a digital gain compensation module. In other words, this DMCA could compensate for temperature variation peak shifts occurring in real-time. As seen in Fig.11, the photopeak position fluctuates by just 2 percent around the reference position, while the ambient temperature ranges from 19°C to 27°C. Therefore, this DMCA can be used on handheld devices for environmental measurements, to provide stable spectra without calibration prior to measurement or using an external radioactive source attached to the detector surface.

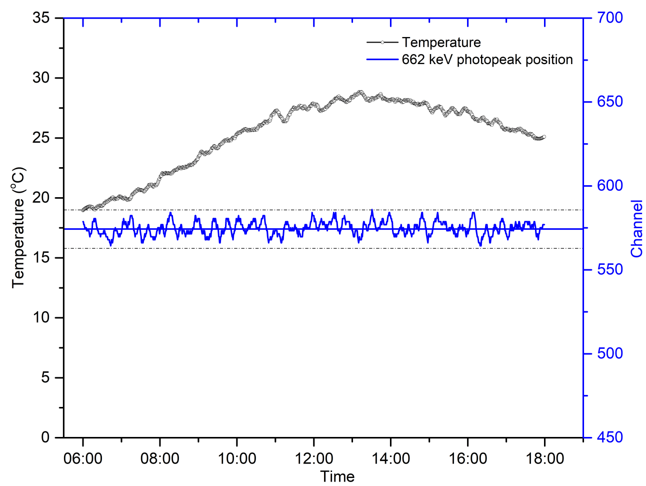

Figure 11: Temperature variations and corresponding corrected positions of the ^{137}Cs photopeak during the test in the open environment. The solid blue line denotes mean value of the corrected peak positions while black dotted lines reflect 2% deviations from this mean value.

4. Conclusion

In this study, a compact, low-cost and flexible FPGA-based DMCA with compatible acquisition and analysis software was presented. The system performance was benchmarked with a 3"×3" NaI(Tl) scintillation detector and compared to a commercial DMCA system. Measurement results at various counting rates indicate that our proposed system can perform well at counting rates up to 100 kcps without much loss in spectral quality. Both pulse analysis and temperature compensation algorithms were successfully configured on the FPGA. Therefore, with an external temperature sensor, this system can act as a reliable stand-alone module for radiological and nuclear security, environmental monitoring, and portable applications, particularly when long-time measurements are needed. In addition, only small amounts of the FPGA's resources were utilized in this work, indicating that this configuration can be extended for a low-cost and small multi-detector system.

5. Acknowledgment

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