# An Improved Wide-Band Referenceless CDR with UP Pulse Selector for Frequency Acquisition

Pham Manh Ha*, Nguyen Huu Tho*, Nguyen Thanh*, Quang Nguyen-The*
*Department of Communications, Le Quy Don Technical University, Hanoi, VIETNAM.
E-mail: pmha@mic.gov.vn, tho.nh@mta.edu.vn, ngthanh1210@yahoo.com, quangnt@mta.edu.vn
Correspondence: Quang Nguyen-The (quangnt@mta.edu.vn)

***Abstract*—This paper presents a wide-band referenceless clock and data recovery (CDR) with a UP pulse selector in frequency acquisition scheme that decreases frequency tracking time. By combining coarse and fine frequency tracking loops, the CDR obtains a capture range from 0.3 Gb/s to 3.2 Gb/s, which is limited only by the operating frequency of the voltage control oscillator (VCO). A digital frequency band selector for the wide-band VCO is presented as well to select an exact frequency band of the VCO. The proposed CDR is implemented in 180 nm CMOS process, achieves the frequency acquisition time of 0.8 $\mu$s with tracking range of 300 MHz and 10-ps peak-to-peak jitter of recovery clock at 3 Gb/s.**

***Index Terms*—clock and data recovery (CDR), referenceless CDR, wide-band, continuous-rate**

## I. Introduction

The referenceless clock and data recovery (CDR) plays a key role in wireline communication applications, such as clock recovery and data retiming. Recently, various referenceless CDR designs have been proposes [1] – [8]. The most significant challenge of a referenceless CDR design is false locking issue while extracting a bit rate of an input data stream. The CDR scheme introduced in [1] uses a dual-loop architecture with a delay locked loop based frequency acquisition. This configuration requires a power-hungry delay line to delay a high speed data and stringent matching between a voltage controlled delay line and a voltage control oscillator (VCO) using the same a voltage controlled line. A digital approach for frequency tracking process is investigated in [2] where a divider-based stochastic reference clock generator is used to generate a sub-harmonic tone from random data. However, the disadvantage of this scheme is that the performance of frequency acquisition process relies on data transition density. Moreover, a small reference frequency can lead to a quite long frequency acquisition time. A simple frequency detection technique that counts the number of consecutive transition edges of the clock/data in a data bit/half of clock period to achieve a bidirectional frequency detection capability, which reduces frequency acquisition time is presented in [3], but it is not a continuous-rate CDR. The CRD scheme suggested in [4] obtains phase and frequency lock by a frequency injection technique, however its requires the 8B10B data encoding. The single loop CDR is investigated in [5, 6] to decrease power consumption and space. In [5], a "phase reset" technique is used to get rid of the frequency tracking loop. However, the relative frequency operating range of the circuit is limited. To overcome this drawback, the single loop CDR in [6] utilizes intrinsic frequency detection capability of the linear half-rate phase detector, but it is a unidirectional frequency detector, where the VCO always starts from its minimum frequency for frequency acquisition operation, thereby increasing frequency acquisition time. CDR schemes introduced in [7, 8] employ a coarse/fine two-step frequency acquisition process to achieve wide-band, bidirectional and continuous-rate frequency detection capability. In [7], two counters for the rising transition of the input data and the sampled data in the coarse-frequency detector (FD) is used for an asynchronous baud-rate sampling scheme with unbalanced frequency detection gain.

This paper proposes an updated version of the frequency acquisition scheme introduced [8]. By using an additional UP pulse selector, the frequency acquisition time of frequency increment tracking process is decreased. The CDR simultaneously obtains wide-band, bidirectional and continuous-rate frequency detection capability. In addition, a frequency band selector for wide-band VCO is adopted. The remainder of this paper is organized as follows. The architecture of the proposed referenceless CDR is introduced in Section II. Next, in Section III, the circuit implementation is described in detail. Section IV provides the experimental results on 180 nm CMOS process followed by conclusions in Section V.

## II. Proposed Architecture

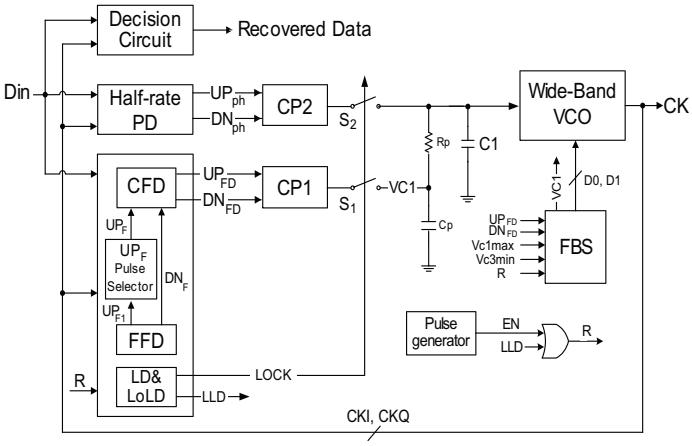


Fig. 1. Block diagram of the proposed referenceless CDR.

The block diagram of the proposed referenceless CDR with UP pulse selector is shown in Fig. 1. The CDR includes a phase locked loop (PLL) and a frequency locked loop (FLL). The PLL consists of a binary phase detector in current-mode logic for high speed [9], a charge_pump1 (CP1), a loop filter, a frequency band selector (FBS) and a ring-VCO. The FLL consist of the proposed FD and a charge_pump2 (CP2) circuit. The frequency tracking scheme implements the coarse/fine two-step frequency acquisition, involves a coarse frequency detector (CFD), a fine frequency detector (FFD), the proposed UP pulse selector, a frequency lock detector (LD) and a loss-of-lock detector (LoLD). An on-chip pulse generator is designed to generate EN signal for resetting the CDR to initial state. The CDR is operating at half rate, and a triple-band VCO having 4 delay stages is employed.

As depicted in Fig. 1, at first, when the EN signal is activated, switch S1 turns on and S2 turns off, the CDR starts a frequency acquisition process. Based on bit rate of the input data, the proposed frequency band selector selects a suitable frequency band for the triple-band VCO by updating the control bits D0, D1. Then, the proposed FD tracks the frequency error between the input data and the output clocks, i.e., CKI and CKQ. When the frequency error is small enough, the LD triggers the LOCK signal to turn off S1 and turn on S2. Then, the PD takes over the acquisition process. When the LoLD detects a variation of the input data rate, it generates an LLD signal to reset the CDR, simultaneously starts a new frequency acquisition process.

## III. CIRCUIT DESCRIPTION

### A. Operation of Frequency Detector

In [7], a coarse/fine frequency acquisition scheme has been used for a referenceless CDR. However, the coarse/fine frequency acquisition loops operate independently. When the FLL starts, the coarse FD functions and the fine FD only works after the coarse FD finishes. As a result, the frequency acquisition time of the CDR is quite long. To solve this problem, the FLL in [8] presented a frequency tracking technique in which the coarse FD and the fine FD work simultaneously as shown in Fig. 2.

$UP_F$ and $DN_F$ signals are the outputs of the FFD, $UP_C$ and $DN_C$ signal are the outputs of the CFD. Two OR-gate and two MUX circuits are used to combine the FFD and the CFD. A D-type flip-flop (D-FF) generates the signal STOP to select appropriate $UP_{FD}$/$DN_{FD}$ that is applied to the CP2 to change the VCO frequency following the input data rate. When half of input data rate is higher than the VCO frequency, the signal STOP arises and the $UP_{FD}$ signal at the ouput of FD becomes

$$\mathrm{UP_{FD}} = \mathrm{UP_C} + \mathrm{UP_F} \tag{1}$$

This means that the frequency updating rate of the frequency increment acquisition FD depends on the pulsewidth of the $UP_C$ and $UP_F$ signal, while the pulsewidth of $UP_F$ signal is directly proportional to the input data rate. Consequently, the efficiency of the combination of the CFD and FFD in [8] is reduced with respect to the increase of the data rate. To overcome this problem, we propose an UP pulse selector for high data rate to achieve shorter frequency acquisition time (Fig. 1). Instead of directly apply the $UP_F$ signal to the CFD, the UP pulse selector is used to extend $UP_F$ pulsewidth for high data rate. This structure allows to increase the frequency changing rate for the frequency increment acquisition process.

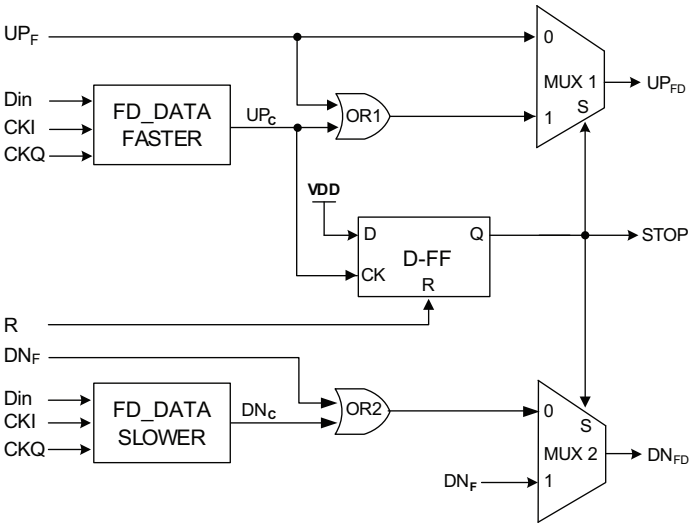


Fig. 2. Block diagram of frequency acquisition process in [8].

### B. The UP Pulse Selector

Fig.3 presents the block diagram of proposed UP pulse selector, which includes an 8-divider, a 2-divider, two 5-bit counters, a MUX, two OR-gate, a NOT-gate and four AND-gate. The STOP signal comes from the CFD and D0, D1 come from the FBS (the operation will be discussed in Section C).

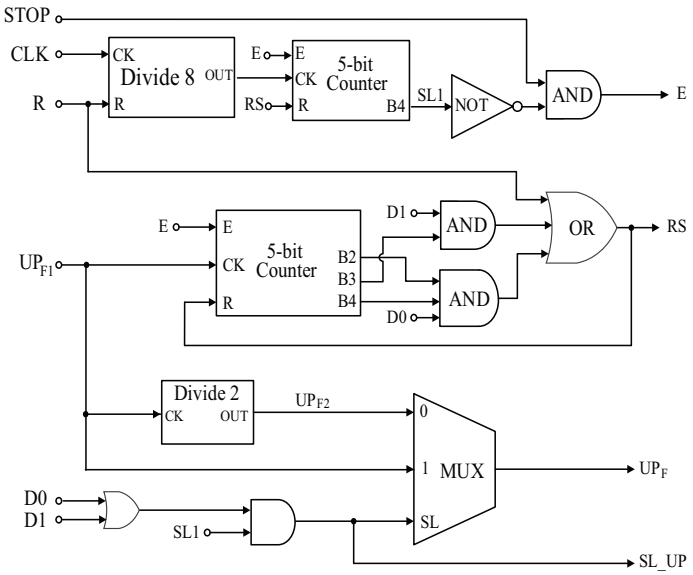


Fig. 3. Block diagram of proposed UP pulse selector.

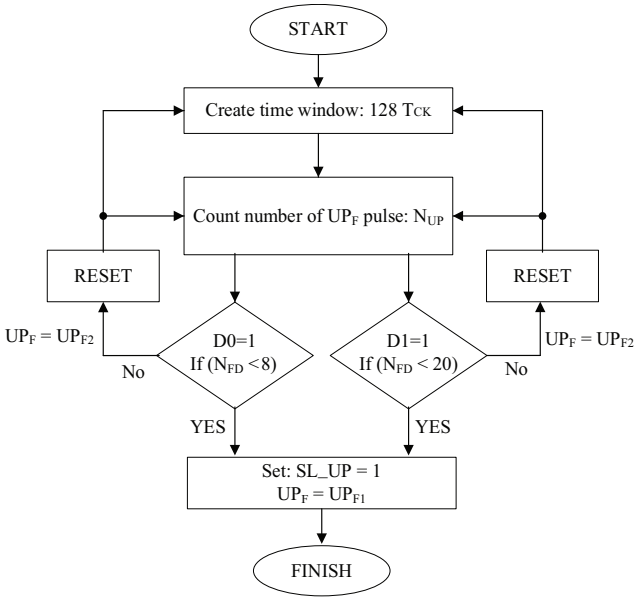


Fig. 4. UP pulse selection algorithm.

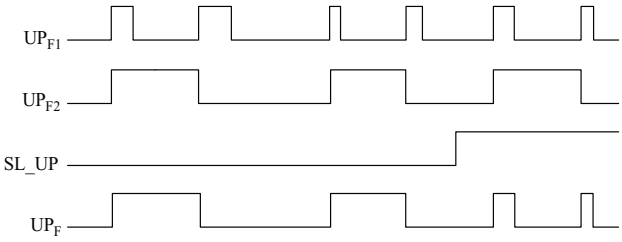


Fig. 5. Timing diagram of UP pulse selector.

The UP pulse selection algorithm for the frequency acquisition process is shown in Fig. 4. As mentioned early, the $UP_F$ pulsewidth is narrow with respect to high data rate and vice versa. For this reason, in this work we only extend $UP_F$ pulsewidth for band 2 (D0 = 1) and band 3 (D1 = 1) among the three bands of the triple-band VCO. The $UP_F$ pulsewidth is extended by a 2-divider ($UP_{F2}$). At the first time of the frequency tracking process, the UP pulse selector creates a timing window of 128 TCK and counts the number of $UP_{F1}$ pulse (output of the FFD) in this timing window ($N_{UP}$). Because the number of $UP_{F1}$ pulses is directly proportional to the frequency error, the $N_{UP}$ is significant and $UP_{F2}$ is selected as output of the UP pulse selector to apply to the CFD ($UP_F$ = $UP_{F2}$). Thus the frequency updating process is sped up. When frequency error decreases, the $N_{UP}$ decreases as well. If $N_{UP}$ is less than 20 while the VCO is operating in band 2 or less than 8 while the VCO is operating in band 3, an SL_UP signal is triggered to turn off the UP pulse selector, the $UP_{F1}$ signal instead of $UP_{F2}$ signal is used as input of the CFD ($UP_F$ = $UP_{F1}$ as shown in Fig. 5). The reason for the need of SL_UP signal is if the $UP_{F2}$ signal is applied constantly to the CFD for frequency acquisition process the frequency change rate of the VCO still stays fast even though the VCO frequency is closely to the half of input data rate. This can cause an error in frequency acquisition process. The VCO frequency could pass the locking point.

A simulation for the FLL in [8] and this work is implemented with same conditions to verify efficiency of the proposed UP pulse selector. The comparison of FLLs in terms of the VCO frequency updating rate is shown in the Table I. With the input data rate of 3 Gb/s, the CP current of 500 $\mu$A and capacitor in loop filter of 1 nF, the control voltage (VC) of the VCO with UP pulse selector increases faster than the case without UP pulse selector. This means that the proposed FLL has faster frequency updating rate, obtains shorter frequency acquisition time.

TABLE I
COMPARISON OF FLLS ABOUT THE VCO FREQUENCY UPDATING RATE.

| **Simulation time (ns)** | 100 | 300 | 500 | 700 | 900 |
|---|---|---|---|---|---|
| **VC without UP pulse selector (mV) [8]** | 530 | 563 | 588 | 623 | 658 |
| **VC with UP pulse selector (mV)** | 538 | 586 | 652 | 710 | 757 |

### C. The Frequency Band Selector

In our work, the wide-band VCO is designed with three operating frequency bands, which is selected by two logic bits D0, D1 as shown in Table II. The VCO's full working frequency range is from 150 MHz to 1.6 GHz, with band 1 from 150 MHz to 820 MHz, band 2 from 800 MHz to 1.24 GHz, band 3 from 1.22 GHz to 1.6 GHz. Fig. 6 depicts the VCO transfer curves for these three bands.

TABLE II
CONTROL LOGIC BITS VERSUS FREQUENCY BANDS OF VCO

| | | **DO** | |
|---|---|---|---|
| | | 0 | 1 |
| **D1** | 0 | Band 1 (150-820)MHz | Band 2 (0.8-1.24)GHz |
| | 1 | Band 3 (1.22-1.6)GHz | N/A |

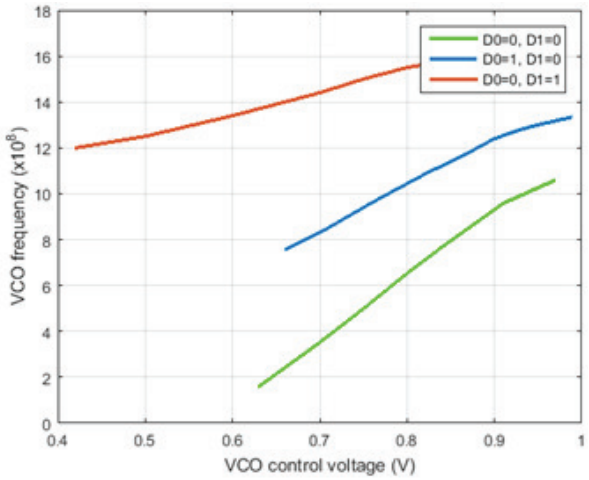


Fig. 6. The VCO tranfer curves.

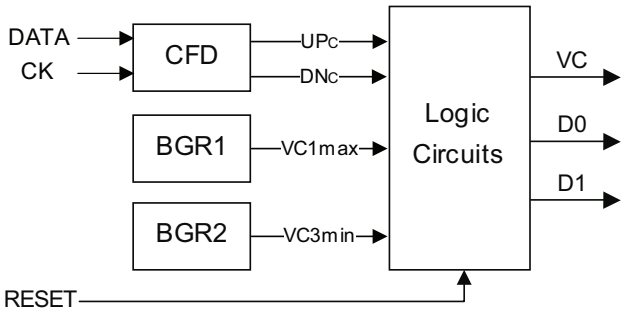


Fig. 7. Frequency band selector for wide-band VCO.

Fig. 7 shows diagram of the frequency band selector for the wide-band VCO. The FBS consists of two band gap reference circuits, BGR1 and BGR2 [10], to generate VC1max and VC3min, respectively; logic circuits with input of UPC, DNC from the CFD and $VC1_{max}$, $VC3_{min}$ from BGRs generate control voltage and two control logic bits D0, D1 that are applied to the VCO.

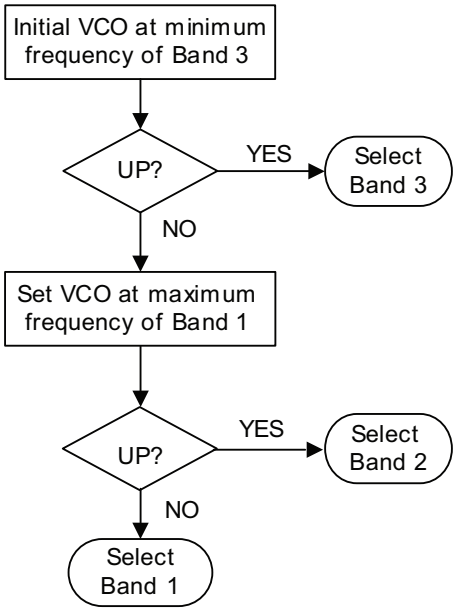


Fig. 8. Frequency band selector for wide-band VCO.

Fig. 8 shows the frequency band selection algorithm for the VCO. The $UP_C$ signal is used to determine the suitable frequency band of the VCO and the $DN_C$ signal is used to create timing windows for checking $UP_C$ existence. At first, the VC is set to $VC3_{min}$ to let the VCO operating at minimum frequency of band 3, D1 = 1. Logic circuits will check existence of $UP_C$ signal. If the $UP_C$ signal arises, the FBS will select band 3 for the VCO. On the contrary, VC will be set to $VC1_{max}$ to the VCO operating at maximum of band 1, D1 = 0 and keep checking existence of $UP_C$ signal. If the $UP_C$ signal absents at the output of CFD circuit, the FBS selects band 1 for the VCO. On the contrary, the FBS selects band 2 for the VCO, D0 is triggered to 1. The FBS completes the frequency band selection for the VCO.

## IV. SIMULATION RESULTS

The proposed referenceless CDR is implemented in a 180 nm CMOS process. The simulation results show that the proposed half-rate CDR successfully recovers with PRBS7 pattern from 300 Mb/s to 3.2 Gb/s.

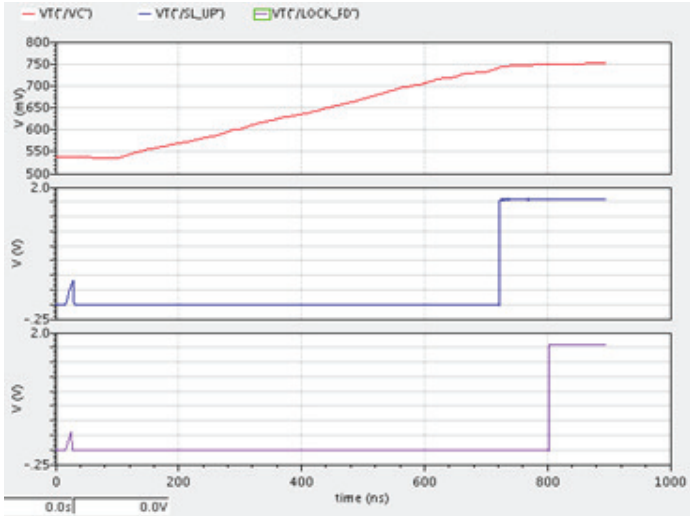


Fig. 9. Operation of UP pulse selector in frequency acquisition process.

Fig. 9 shows the frequency acquisition process of the proposed CDR with the UP pulse selector at input data rate of 3 Gb/s. At first, the FBS functions to select band 3 for the VCO, the VCO starts working from 1.22 GHz. The UP pulse selector extends $UP_F$ pulsewidth to increase the frequency updating speed of the VCO. When the VCO frequency reaches to 1.49 GHz, the SL_UP signal is triggered to stop the UP pulse selector. After that, the FLL locks at 1.499 MHz of the VCO frequency with the frequency acquisition time of 0.8$\mu$s, finishes frequency tracking process and takes over to phase tracking process.

Fig. 10. Jitter performance of recovered clock and data at 3 Gb/s.

Fig. 10 shows the jitter of the recovered clock and data at 3 Gb/s of input data rate. The CDR obtains a peak-to-peak jitter of 10 ps and 12 ps, respectively. Table III compares performance of the proposed scheme to that of other works, revealing the resulted outstanding acquisition time.

TABLE III
COMPARISON OF FLLS ABOUT THE VCO FREQUENCY UPDATING RATE.

| | **[3]** | **[6]** | **[8]** | **This work** |
|---|---|---|---|---|
| Technology (nm) | 180 CMOS | 130 | 80 CMOS | 180 CMOS |
| Supply (V) | 1.8 | 1.5 | 1.8 | 1.8 |
| Data rate (Gb/s) | 0.2–3.2 Half-Rate | 0.4–2.5 Half-Rate | Half-Rate (only FLL) | 0.3–3.2 Half-Rate |
| FD type | Bidirectional | Unilateral | Bidirectional | Bidirectional |
| Continuous-rate | No | Yes | Yes | Yes |
| $\text{Jitter}_{\text{p-p}}$ (ps) | 11@3Gb/s | 53 | N/A | 10@3Gb/s |
| Freg. acquisition time ($\mu$s) | 12.9 | 17 | 1.73 | 0.8 |

## V. CONCLUSION

The proposed referenceless 300 Mb/s to 3.2 Gb/s rate CDR with UP pulse selector is implemented in 180 nm CMOS process. The FD achieves wide-band, bidirectional, continuous-rate frequency detection capability and an unlimited frequency acquisition range in which only depends on the VCO operating frequency range. It decreases the frequency acquisition time to 0.8 $\mu$s with tracking range of 300 MHz in simulation, outperforming other published schemes.

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