Journal Pre-proofs

Regular paper

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PII: S1434-8411(19)31317-2
DOI: https://doi.org/10.1016/j.aeue.2019.152999
Reference: AEUE 152999

To appear in: *International Journal of Electronics and Communications*

Received Date: 22 May 2019
Accepted Date: 13 November 2019

Please cite this article as: H.L. Duc, T.K. Phuong Dinh, V-P. Hoang, D.M. Nguyen, All-Digital Background Calibration of Gain and Timing Mismatches in Time-Interleaved ADCs Using Adaptive Noise Canceller, *International Journal of Electronics and Communications* (2019), doi: https://doi.org/10.1016/j.aeue.2019.152999

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All-Digital Background Calibration of Gain and Timing Mismatches in Time-Interleaved ADCs Using Adaptive Noise Canceller

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Received: date / Accepted: date

Abstract This paper proposes a novel all-digital background calibration technique for gain and timing mismatches in Time-Interleaved Analog-to-Digital Converters (TIADCs) using adaptive noise canceller (ANC). The error signals due to the gain and timing mismatches are expressed in linear regression terms, producing the estimation problem of ANC. The gain and clock skew coefficients are estimated by maximizing the output signal-to-noise ratio in ANC system. The correction is simple by subtracting the re-constructed errors from the TIADC output. The proposed calibration technique eliminates the input spectrum constants as well as removes high-pass filters, which are required in the conventional free-band based calibration technique. In order to validate the proposed approach, simulations are carried out for an 11-bit, 2.7 GS/s four-channel TIADC for various input signals. Results show that the proposed calibration produces excellent performance in terms of mismatch distortion suppression. It achieves the SNDR and SFDR improvement of 19 dB and 49 dB, respectively. Moreover, the synthesized design with hardware co-simulation on Xilinx Kintex-7 field-programmable gate array (FPGA) platform consumes only 7.36% of the hardware resources of the FPGA chip and reduces the mismatch tone level up to −87 dB.

Keywords All-digital calibration, TIADCs, FPGA implementation, adaptive noise canceller.

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1 Introduction

Modern data communication systems such as full-band capture cable TV tuner transmissions, baseband optical communication and satellite communication receivers require the use of high-speed, high resolution and energy efficient analog-to-digital converters (ADCs). A time-interleaved ADC (TIADC) exploiting multiple individual ADCs operating in parallel can meet this requirement [1, 2]. In such a time-interleaved structure, sub-ADCs sequentially carry out time-shifted analog-to-digital conversion of an analog signal, following a round-robin fashion. The time-interleaving technique is not only a mean of increasing the conversion rate but also affords in power-speed tradeoff. It can be used to extend the efficiency of the ADCs to the high frequencies, which is required in modern embedded systems and Internet of Things (IoT) applications [3, 4]. Unfortunately, TIADC performance suffers from channel mismatches consisting of offset, gain and timing mismatches among sub-ADCs. The severe effect of these channel mismatches is to produce frequency aliases on the output signal, hence significantly degrading the Signal-to-Noise-and-Distortion Ratio (SNDR) and Spurious-Free Dynamic Range (SFDR) performance of TIADCs. In practice, the mismatch among the individual ADCs is mostly unknown since the imperfections of each sub-ADC are introduced by process, voltage, and tempera-

ture (PVT) variations. Therefore, in order to enhance the TIADC performance, the mismatch errors in TIADCs must be continuously tracked and mitigated by calibration techniques.

Recently, the calibration techniques can be categorized by mixed-signal and all-digital calibrations [5]. Mixed-signal calibration techniques [2, 6–10] mitigate the clock skew effects by employing an analog variable delay line (VDL) in each sub-ADC's clock path, while fully digital approaches use post digital signal processing (DSP) to directly compensate the TIADC outputs [5, 11–18]. Although an analog correction exhibits good performance, it suffers from PVT variations and the additional jitter introduced by the VDL [19]. Digital calibration is unaffected to PVT variations and takes the advantages of scaled CMOS technologies, hence attracting recent interest of both the circuit design and the signal processing communities.

Authors in [13, 15, 20] developed the timing mismatch calibration mechanisms for an arbitrary number of interleaved channels by using a digital synthesis filter bank in the correction phase, consisting of more than two digital adaptive filters appending to the sub-ADC outputs to mitigate the effects of timing mismatch. Rigorously, such digital correction system requires high complexity level (or large amount of computation resource), hence dissipates high power and costs large chip area. The approaches using digital synthesis filter bank are actually not good candidates in multi-GS/s ADC designs. Currently, there are two well-known estimation classes: *cross-correlation based estimation* [5, 11, 12, 21, 22] and *free-band based estimation* [13–15, 18]. In the first class, techniques compute the cross-correlation function between the errors due to channel mismatches and the compensated signals. The resulted cross-correlation is minimized in order to estimate the channel mismatches. In the second class, calibration assumes the distortions to appear in an out-of-band region where no signal component is present. It has owned the following limitations: the input signal is slightly oversampled; there exists an out-of-band region effected only by the error spectra; and the location of the mismatch band is known beforehand in order to design high-pass filter. In other words, it puts high constraints on input spectrum such that all image spectra due to timing mismatch must be inside the mismatch band in order to make an accurate estimation, which can be referred to as *semi-blind* calibration.

In this paper, we propose the novel estimation technique of gain and timing mismatches based on Adaptive Noise Canceller (ANC), which maximizes the output signal-to-noise ratio. Our approach eliminates the limitations of the aforementioned mismatch band based calibration such as relaxing the pre-existence of an out-of-band region and removing the high-pass filter, which can reduce the complexity of hardware implementation. The digital correction is simple by mismatch error subtraction from the TIADC output. The performance comparison between the proposed calibration and the cross-correlation based calibration, is also analyzed. The hardware design of the proposed calibration is validated on the field-programmable gate array (FPGA) platform.

The rest of the paper is organized as follows. Section 2 analyzes the system model. Section 3 presents the ANC based calibration technique. In order to show the efficiency of the proposed calibration, Section 4 analyzes simulation and experimental results with FPGA validation. Finally, conclusions are included in Section 5.

2 System Model Analysis

In this section, the linear approximation of the time-varying errors $e[n]$ due to the gain and timing mismatches among sub-ADCs, is analyzed. The channel mismatch coefficient vectors of $\{\mathbf{c}_g, \mathbf{c}_r\}$ are formulated. These coefficients are expected values of the estimated parameters in the estimation techniques.

A commonly known model of an M-channel TIADC in the presence of gain and timing mismatches across the multiple sub-ADCs is shown in Fig. 1 [18]. The m-th channel is characterized by the gain g_m and the timing mismatch $r_m T_s$ for $m = 0, 1, \ldots, M-1$, where r_m presents the timing mismatch related to the overall sampling period T_s. Each channel sample of the input signal $x(t)$ is multiplied by g_m at $(nM+m)T_s + r_m T_s$, resulting in a sequence $y_m[n]$. The TIADC output sequence is formed by combining the output of sub-ADCs using a multiplexer (MUX). Consequently, the effective sampling period of $y[n]$ is T_s, which ideally makes the

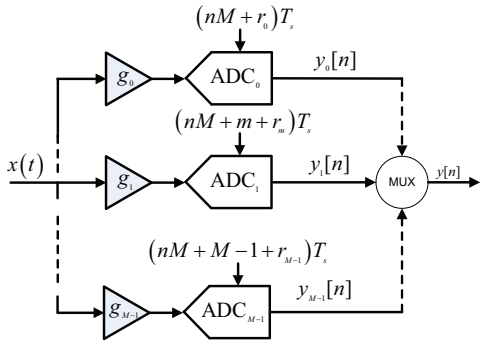
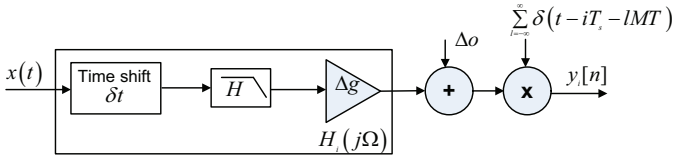


Fig. 1: An M-channel TIADC with gain and timing mismatches.



TIADC equivalent to an ADC clocked at a sampling rate of $f_s = \frac{1}{T_s}$.

Assuming the input signal $x(t)$ is slightly oversampled and bandlimited ($X(j\Omega) = 0$ for $|\Omega T_s| \geq \pi$), the discrete-time Fourier transform (DFT) of the output $y[n]$ can be expressed as [18, 23]

$$Y\left(e^{j\omega}\right) = \sum_{k=0}^{M-1} X\left(e^{j(\omega - \frac{2\pi k}{M})}\right) \breve{H}_k\left(e^{j(\omega - \frac{2\pi k}{M})}\right), \tag{1}$$

where

$$\begin{aligned} \breve{H}_k(e^{j\omega}) &= \tfrac{1}{M} \sum_{m=0}^{M-1} g_m e^{r_m H_d(e^{j\omega})} e^{-jk\frac{2\pi}{M}m}, \\ H_d\left(e^{j\omega}\right) &= \quad j\omega, \text{for} - \pi < \omega < \pi, \end{aligned} \tag{2}$$

and $H_d\left(e^{j\omega}\right)$ is the frequency response of an ideal derivative filter [24]. $X\left(e^{j\omega}\right)$ is the discrete-time spectrum of the sampled input $x[n] = x(t)|_{t=nT_s}$.

Typically, let us assume that the timing skews r_m are small and by exploiting the first-order Taylor's series approximation, the frequency response of the derivative filters can be expressed as

$$e^{jr_m H_d(e^{j\omega})} \approx 1 + r_m H_d(e^{j\omega}). \tag{3}$$

Replacing (2) into (3) gives

$$\breve{H}_k(e^{j\omega}) = G_k + R_k H_d\left(e^{j\omega}\right). \tag{4}$$

where

$$\begin{aligned} G_k &= \tfrac{1}{M} \sum_{m=0}^{M-1} g_m e^{-jk\frac{2\pi}{M}m} \\ R_k &= \tfrac{1}{M} \sum_{m=0}^{M-1} g_m r_m e^{-jk\frac{2\pi}{M}m}. \end{aligned} \tag{5}$$

By taking the inverse DFT of (1) and assuming $G_0 \approx 1$, Vogel *et al.* in [18] analyzes the effect of time-varying errors by presenting the output $y[n]$ in terms of two components as

$$y[n] = x[n] + e[n], \tag{6}$$

where $x[n]$ is a uniformly sampled version of the incoming signal $x(t)$. The error signal $e[n]$ contains spurious terms due to gain and clock skew mismatches that can be respectively expressed as a sum of two following inner-product components.

$$e[n] = \mathbf{c}_g^T \mathbf{x}_{g,n} + \mathbf{c}_r^T \mathbf{x}_{r,n}, \tag{7}$$

where

$$\begin{aligned} \mathbf{x}_{g,n} &= \quad \mathbf{m}_n x[n], \\ \mathbf{x}_{r,n} &= \mathbf{m}_n \left(h_d[n] * x[n]\right). \end{aligned} \tag{8}$$

$h_d[n]$ denotes the impulse response of the ideal derivative filter that is the inverse DFT of $H_d\left(e^{j\omega}\right)$. The modulation vector $\mathbf{m}_n$ is expressed as

$$\begin{aligned} \mathbf{m}_n = \big(&2\cos\left(1\tfrac{2\pi}{M}n\right), -2\sin\left(1\tfrac{2\pi}{M}n\right), \ldots, \\ &2\cos\left(k\tfrac{2\pi}{M}n\right), -2\sin\left(k\tfrac{2\pi}{M}n\right), \ldots, \\ &2\cos\left(\left(\tfrac{M}{2}-1\right)\tfrac{2\pi}{M}n\right), -2\sin\left(\left(\tfrac{M}{2}-1\right)\tfrac{2\pi}{M}n\right), (-1)^n\big)^T, \end{aligned} \tag{9}$$

where T notates the matrix transpose operator. The gain and timing mismatch coefficients vectors $\mathbf{c}_g, \mathbf{c}_r$ with the size of $(M-1)$-by-1 are defined in terms of the real and imaginary parts of the parameters $\{G_k, R_k\}$ as follows:

$$\begin{aligned} \mathbf{c}_g = (&\text{Re}\{G_1\}, Im\{G_1\}, \ldots, \\ &Re\{G_{\frac{M}{2}-1}\}, Im\{G_{\frac{M}{2}-1}\}, (-1)^n)^T \end{aligned} \tag{10}$$

$$\begin{aligned} \mathbf{c}_r = (&\text{Im}\{R_1\}, Im\{R_1\}, \ldots, \\ &Re\{R_{\frac{M}{2}-1}\}, Im\{R_{\frac{M}{2}-1}\}, (-1)^n)^T \end{aligned} \tag{11}$$

Obviously, when the channel mismatch coefficient vectors $\mathbf{c}_g$ and $\mathbf{c}_r$ are estimated, a compensated signal can be obtained by eliminating the second term in the right side of (6).

3 Proposed Calibration Technique

This section proposes the adaptive calibration using ANC, where the instant time coefficients $\mathbf{c}_n = \{\mathbf{c}_{g,n}, \mathbf{c}_{r,n}\}$ are adaptive based on the feed-back loop such that the output signal-to-noise ratio maximizes. It is worth noting that $\mathbf{c}_{g,n}$ and $\mathbf{c}_{r,n}$ are the estimated mismatch coefficient vectors of $\mathbf{c}_g$ and $\mathbf{c}_r$ at the instant time of n, respectively.

The error signal due to gain and timing mismatches is linearly presented in terms of the mismatch coefficients as expressed in (7). Using (6) and (7), we can write

$$\begin{aligned} y[n] &= \underbrace{\left[\mathbf{x}_{g,n}^T \; \mathbf{x}_{r,n}^T\right]}_{\mathbf{u}_n^T} \underbrace{\begin{bmatrix}\mathbf{c}_g \\ \mathbf{c}_r\end{bmatrix}}_{\mathbf{c}} + x[n] \\ &= \quad \mathbf{u}_n^T \mathbf{c} + x[n]. \end{aligned} \tag{12}$$

It is worthy noting that the mismatch error signal is the linear regression term $\mathbf{u}_n^T \mathbf{c}$ constructed by a linear filter, and $x[n]$ represents the signal component needed to be estimated. Therefore, the estimation problem is referred to as an adaptive noise canceller presented in [24] and shown in Fig. 2. The output of the linear filter is expressed by

$$\hat{e}[n] = \mathbf{u}_n^T \mathbf{c}_{n-1}, \tag{13}$$

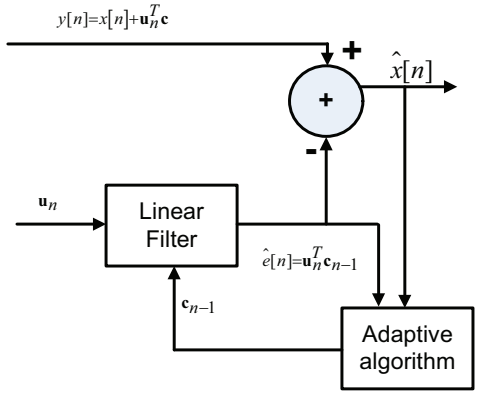


Fig. 2: Digital estimation based on Adaptive Noise Canceller (ANC).

where $\mathbf{c}_{n-1}$ is the estimated mismatch coefficient vector of $\mathbf{c}$ at the instant time of $n-1$. It can be expressed by

$$\mathbf{c}_{n-1} = \begin{bmatrix} \mathbf{c}_{g,n-1} \\ \mathbf{c}_{r,n-1} \end{bmatrix}, \tag{14}$$

where $\mathbf{c}_{g,n-1}$ and $\mathbf{c}_{r,n-1}$ are the estimated mismatch coefficient vectors of $\mathbf{c}_g$ and $\mathbf{c}_r$ at the instant time of $n-1$, respectively. By feeding the output feedback to the linear filter and then adjusting the coefficients of the linear filter via an LMS adaptive algorithm to minimize total system output power, an output $\hat{x}[n] = x[n] + \left(\mathbf{u}_n^T\mathbf{c} - \mathbf{u}_n^T\mathbf{c}_{n-1}\right)$ that is best fit in the least squares estimation of the signal $x[n]$ is produced. Thus, the system output serves as the error signal for the adaptive process as shown in Fig. 2.

Let us assume that the input signal $x[n]$ is a Wide-Sense Stationary (WSS). Then, the input signal $x[n]$ is uncorrelated to both the error signal $e[n] = \mathbf{u}_n^T\mathbf{c}$ and the error estimate $\hat{e}[n] = \mathbf{u}_n^T\mathbf{c}_{n-1}$. As shown in Fig. 2, we have

$$\begin{aligned} \hat{x}[n] &= y[n] - \mathbf{u}_n^T\mathbf{c}_{n-1} \\ &= x[n] + (e[n] - \hat{e}[n]). \end{aligned} \tag{15}$$

Taking square root of both sides of (15), we have

$$\hat{x}^2[n] = x^2[n] + (e[n] - \hat{e}[n])^2 + 2x[n](e[n] - \hat{e}[n]). \tag{16}$$

Taking expectation of both sides and noting that the input signal is uncorrelated with the error signal, i.e., $E\{x[n](e[n] - \hat{e}[n])\} = 0$, we have

$$E\left\{\hat{x}^2[n]\right\} = E\left\{x^2[n]\right\} + E\left\{(e[n] - \hat{e}[n])^2\right\}. \tag{17}$$

Obviously, the output noise power $E\left\{(e[n] - \hat{e}[n])^2\right\}$ is minimized when the linear filter is adjusted to minimize the output power $E\left\{\hat{x}^2[n]\right\}$. Therefore, minimizing the total output power maximizes the output signal-to-noise ratio. The coefficients can be derived by an adaptive LMS algorithm as follows.

$$\mathbf{c}_n = \mathbf{c}_{n-1} - \frac{1}{2}\mu\frac{\partial\hat{x}^2[n]}{\partial\mathbf{c}_{n-1}}. \tag{18}$$

where μ is the step-size. Using (15) and (18), the updating equation (18) can be written by

$$\mathbf{c}_n = \mathbf{c}_{n-1} + \mu\mathbf{u}_n^T\left(y[n] - \mathbf{u}_n^T\mathbf{c}_{n-1}\right) \tag{19}$$

In order to run the adaptive algorithm expressed in (19), the regression vector $\mathbf{u}_n$ is required. From (8) and (12), $\mathbf{u}_n$ is calculated based on the unknown input signal $x[n]$. In blind calibration and in order to get more accurate estimations of channel mismatch coefficients, we use the first compensated signal $\overline{x}[n]$ instead of $x[n]$ in (8) to compute $\mathbf{u}_n$ in (12) more accurately.

Fig. 3 shows the proposed ANC-based calibration technique consisting of the digital correction and estimation steps. In the digital correction step, the estimated error signal $\overline{e}[n]$ is subtracted from the distorted TIADC output $y[n]$ in order to produce the corrected signal $\hat{x}[n]$. In the estimation step, the desired coefficients of (10) and (11) are derived from the updating equations in (19) where $\mathbf{u}_n$ is computed from $\overline{x}[n]$ as labeled in Fig. 3.

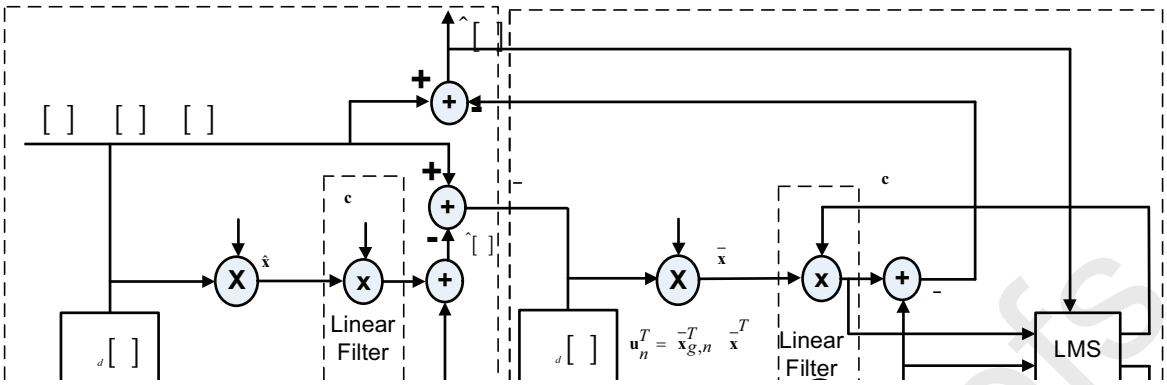
4 Simulation and Experimental Results

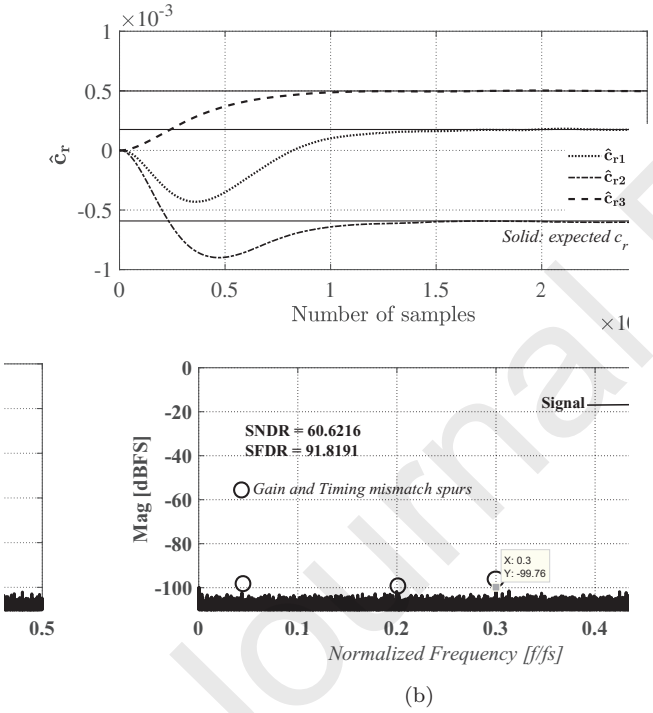
4.1 Simulation Results

4.1.1 Performance Analysis

In order to verify the efficiency of the proposed blind background calibration technique, simulations are carried out for a 11-bit, 2.7 GS/s four-channel TIADC. The derivative FIR filter is designed with 33 taps. In order to eliminate the influence of truncation error, the coefficients of this FIR filter are obtained by multiplying the exact coefficients by Hanning window. μ is taken as $\mu_g = 2^{-13}$ and $\mu_r = 2^{-15}$ for gain and clock skew coefficient estimation.

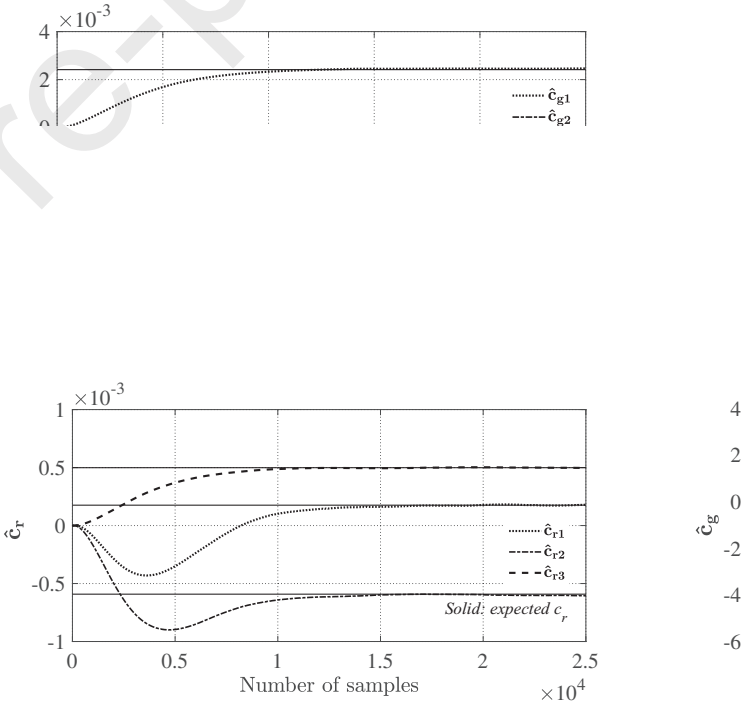
We first investigate the performance of the proposed calibration for the single tone input at $0.45f_s$. Gain and timing mismatches are modeled as Gaussian distribution with zero mean and standard deviations of $\delta_g = 0.02$ and $\delta_t = 0.5$ ps, respectively. We observe a significant reduction in the distortion tones when applying the proposed calibration, as shown in Fig. 4. The





(b)

Fig. 4: Spectra of the TIADC output for single tone input $f_{in} = 0.45 \times f_s$: (a) Before and (b) after the proposed calibration.



(b)

Fig. 5: Time evolution of the channel mismatch coefficients: (a) $\mathbf{c}_g$. (b) $\mathbf{c}_r$.

proposed calibration achieves the SNDR and SFDR improvement of 19 dB and 49 dB, respectively. Fig. 5 illustrates the convergence speed of timing and gain mismatch coefficient estimation. The adaptation loop converges after 20K samples (or 7.4 μs). Fig. 6 shows the SNDR and SFDR performance versus the various values of δ_t for the single-tone input at $0.45 f_s$ and $\delta_g = 0.01$. Obviously, SNDR and SFDR without calibration ac-

cordingly degrade with the increment of δ_t. With the proposed calibration technique, SNDR and SFDR are improved significantly over the simulated clock skews. There is a drop of the achieved SFDR at high clock skews because the first-order Taylor's series is used to provide the clock skew linearization proximate presentation in (3). Moreover, the TIADC output $y[n]$ is used instead of $x[n]$ to approximately compute $\mathbf{x}_{g,n}$ and $\mathbf{x}_{r,n}$ in the correction as illustrated in Fig. 3. These approximations become less accurate when the clock skews increase because the distortion level rises. Given $\delta_g = 0.01$ and $\delta_t = 10$ ps, the proposed calibration obtains the improvement of 35 dB and 75 dB for SNDR and SFDR, respectively, which shows its good efficiency.

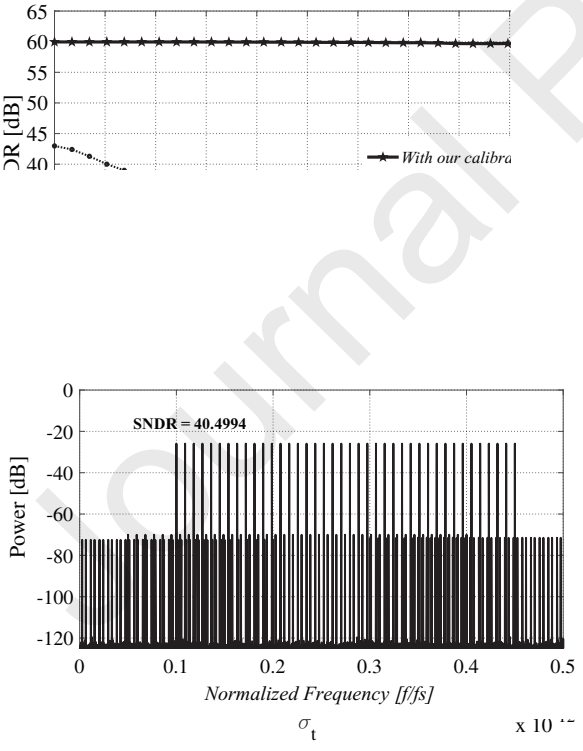
We have further evaluated the efficiency of the proposed calibration for a bandpass multitone input signal that is bandlimited to the bandwidth of $[0.1f_s, 0.45f_s]$. The standard deviation of gain and timing mismatches

nificantly reduced after calibration, hence obtaining the SNDR improvement of 30.69 dB.

The performance of the proposed calibration is also validated for a 16 quadrature amplitude modulation (16-QAM) input signal with 10 MHz bandwidth at the carrier frequency of $0.29f_s$. In order to make pulse shaping, a relatively long FIR square root raised cosine filter with a roll-off factor of 0.3 is used. Fig. 8 shows the obtained results. By employing the proposed calibration, all spurious errors due to gain and timing skew are mostly suppressed. Fig. 9 shows the effectiveness of distortion suppression of the proposed calibration for higher bandwidth of the 16-QAM signal. Again, by applying calibration, the distortion is significantly reduced to noise floor.

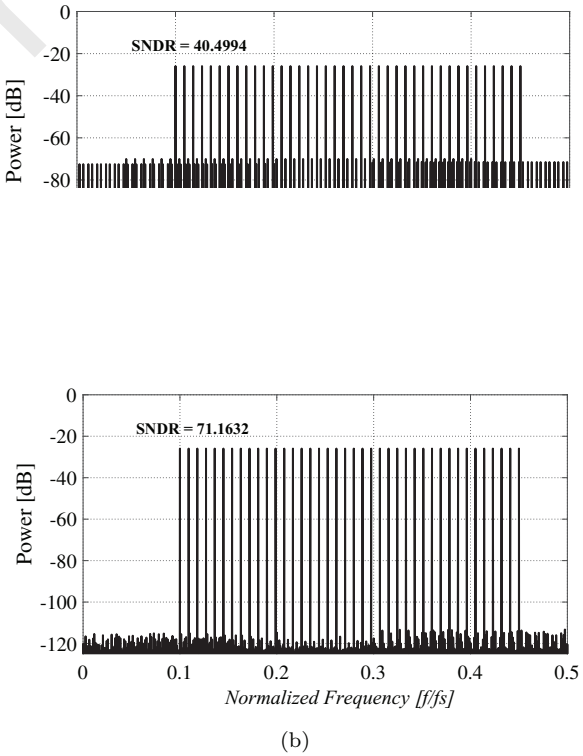
4.1.2 Performance Comparison with Related Works

According to our best knowledge, the prior works [12



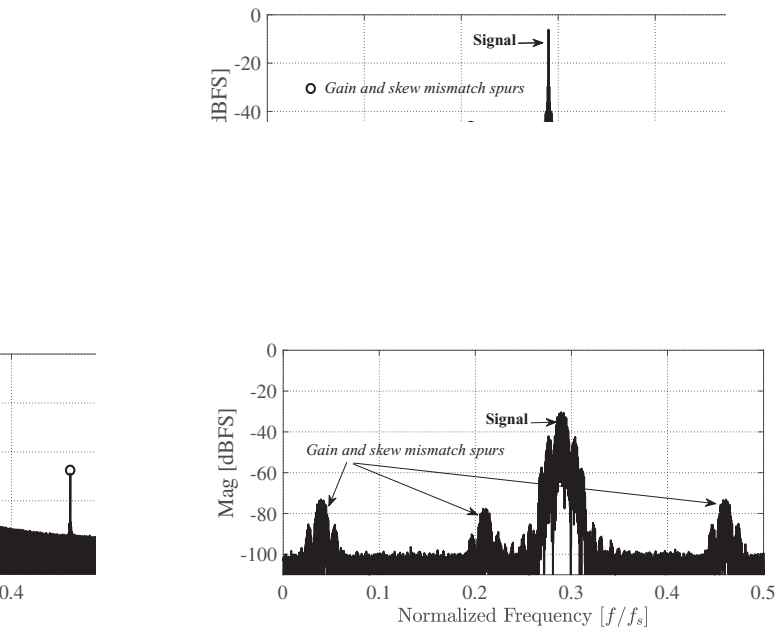
(b)

Fig. 6: SNDR and SFDR performance vs. clock skews for $\delta_g = 0.01$: (a) SNDR; (b) SFDR.



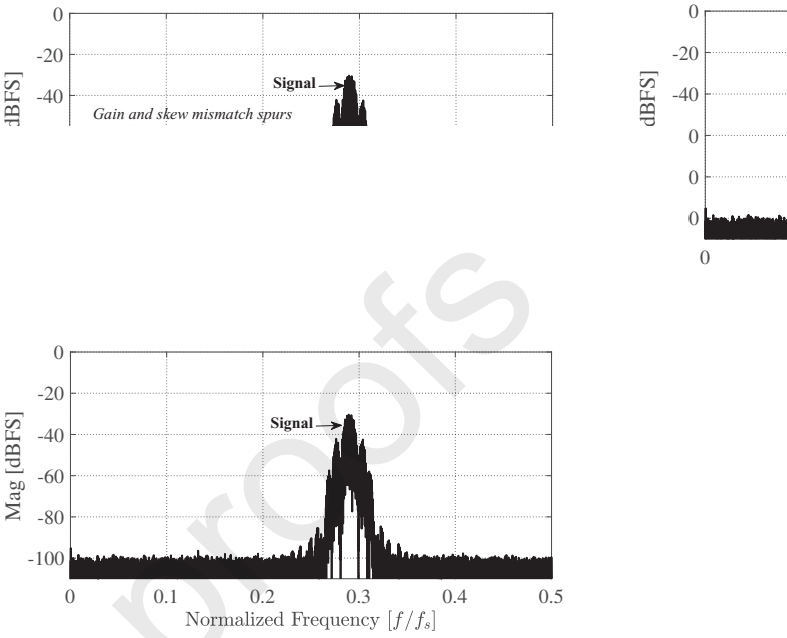
(b)

Fig. 7: Output spectra for the band-limited bandpass multitone input: (a) Before calibration; (b) After calibration.



(b)

Fig. 8: The output spectra for the 16-QAM signal with a carrier frequency of $0.29f_s$ and 10 MHz bandwidth: (a) Without, and (b) with calibration.



(b)

Fig. 9: The output spectra for the 16-QAM signal with a carrier frequency of $0.29f_s$ and 100 MHz bandwidth: (a) Without, and (b) with calibration.

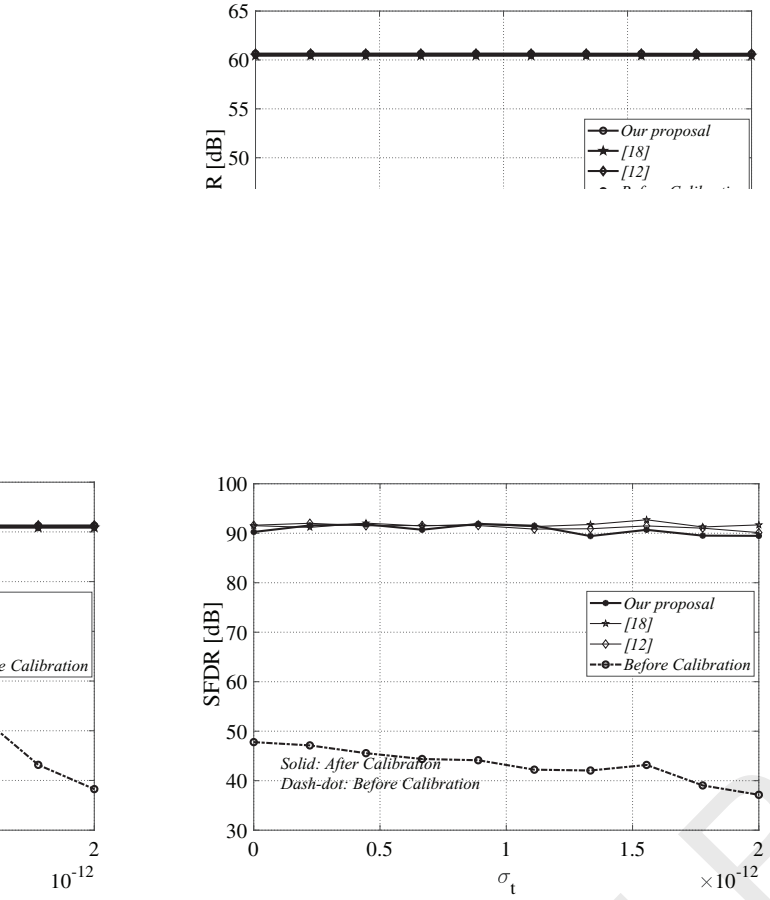
lution and the prior works, where simulation is executed for single-tone input at different frequencies with $\delta_g = 0.01$ and $\delta_t = 0.5$ ps. It is worthy noting that proposed calibration shows almost the same good performance as the above mentioned techniques in terms of the achieved SNDR and SFDR. The SNDR and SFDR performance comparison is evaluated with various clock skews. Fig. 10 shows the achieved results. After calibration, three calibration techniques show the same good performance in terms of the obtained SNDR of 60 dB and SFDR of 90 dB over different clock skews.

Table 1: Simulated SNDR and SFDR performance comparison.

Frequency (MHz)		**718**	**855**	**990**	**1169**
SNDR without cal. (dB)		41.572	41.488	41.397	41.264
SNDR with cal. (dB)	[18]	60.590	60.577	57.165	60.492
	[12]	60.687	60.686	60.683	60.686
	Our approach	60.686	60.664	60.658	60.663
SFDR without cal. (dB)		43.852	43.742	43.630	43.486
SFDR with cal. (dB)	[18]	85.71	92.394	91.903	92.464
	[12]	92.851	92.894	93.130	92.727
	Our approach	91.696	92.394	91.903	92.464

We next analyze the conversion speed results of these compared calibration techniques. Fig. 11 illustrates the analysis results for one single-tone input at frequency of $0.45f_s$, and $\delta_g = 0.01$ and $\delta_t = 0.5$ ps. We observe that SNDR gets saturation region after 20-K samples for the compared techniques, leading to the same convergence speed.

As a result, the proposed calibration provides the same performance as the compared techniques. There are main differences among these approaches. The proposed solution does not require the exist of the out-of-band region, relaxing the input spectrum constraints and removing the high pass filter, whereas the calibration in [18] puts high constraints on the input spectrum in order to design high pass filters. Hence, it can reduce hardware cost compared to the calibration in [18]. The calibration technique in [12] uses cross-correlation between some pseudo-signals and the compensated signals in order to estimate the channel mismatch coefficients, meanwhile the proposed calibration employs ANC-based estimation technique.



(b)

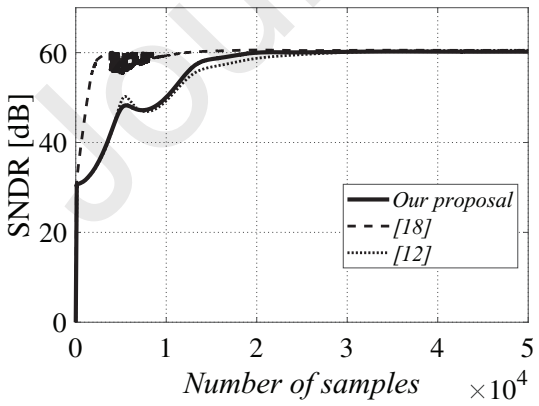
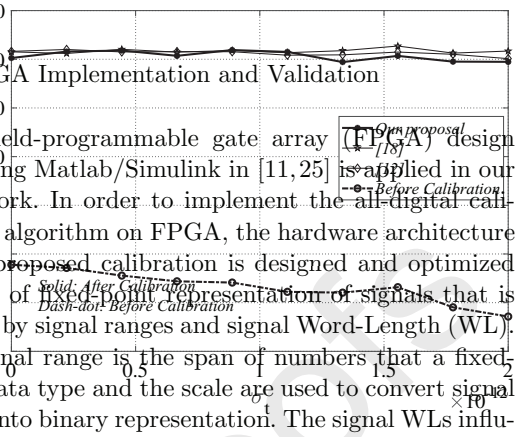


Fig. 11: Time evolution of SNDR during calibration.



4.2 FPGA Implementation and Validation

A field-programmable gate array (FPGA) design flow using Matlab/Simulink in [11, 25] is applied in our framework. In order to implement the all-digital calibration algorithm on FPGA, the hardware architecture of the proposed calibration is designed and optimized in term of fixed-point representation of signals that is defined by signal ranges and signal Word-Length (WL). The signal range is the span of numbers that a fixed-point data type and the scale are used to convert signal values into binary representation. The signal WLs influence on SNDR and SFDR performance metrics of the calibration system. In the optimal fixed-point (OFxp) hardware model, its parameters need to be optimized such as the order of FIR filters and the signal WLs. Fig. 12 illustrates SNDR and SFDR performance versus the number of FIR taps. Obviously, the optimal number of FIR taps is 33 at which the performance saturates. Fig. 13 presents SNDR and SFDR performance versus the number of bits (or WL) assigned to the compensated TIADC output. As can be seen, the optimal values of WL of the compensated TIADC output is 12 bits in order to get the best trade-off between the performance and hardware cost.

Fig. 14 shows the optimal fixed-point (OFxp) hardware architecture of the proposed calibration, processing real time signal data in sample-by-sample manner. The z^{-k} blocks are delayed/pipeline registers. The notation of sfix9_En11 presents a 9-bit signed fixed point data type with a Fraction Length (FL) or fractional bits of 11 [5]. The delays of all signal datapaths are made suitable. The pipeline registers are inserted to reduce the combinational path length and improve the overall working frequency and throughput. The latency between the distorted output and the compensated output is 32 clock cycles.

The above Ofxp hardware architecture is converted into the Hardware Description Language (HDL) model using MATLAB HDL Coder toolbox. In order to reduce the sensitivity to digital truncation errors, the compensated TIADC output is presented in the 12-bit format. The proposed calibration was validated on a Xilinx FPGA board using the FPGA in the loop (FIL) simulation and Xilinx Vivado HL System Edition tool. Fig. 15 shows the testbench configuration for our FPGA implementation consisting of Xilinx Kintex-7 KC705 FPGA evaluation board, JTAG USB cable and PC. The hardware co-simulation with FIL enables to use an FPGA as a simulation device inside a MATLAB Simulink design. This configuration accelerates the simulation process,

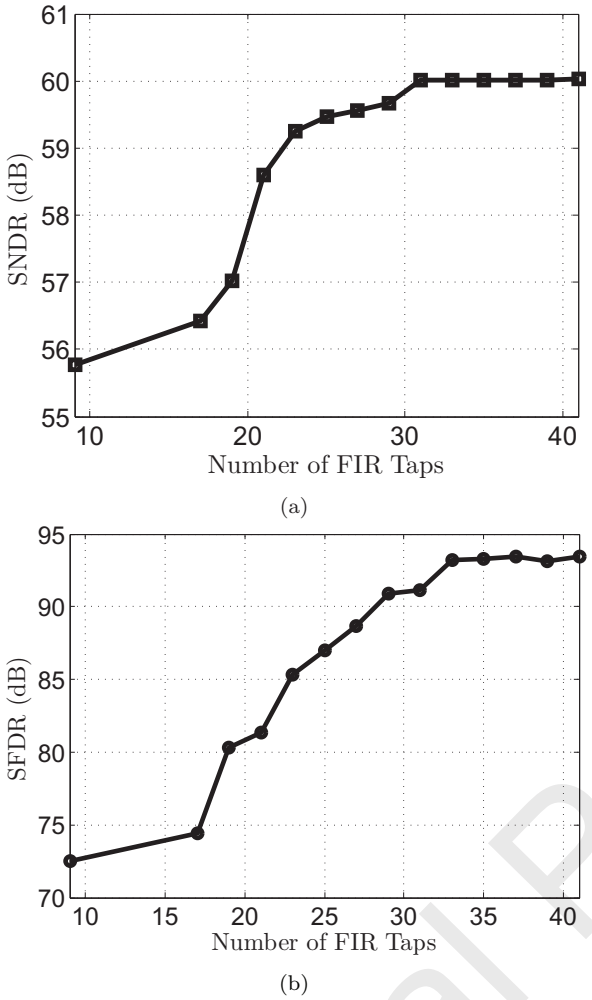


Fig. 12: SNDR and SFDR vs. Number of FIR taps: (a) SNDR. (b) SFDR.

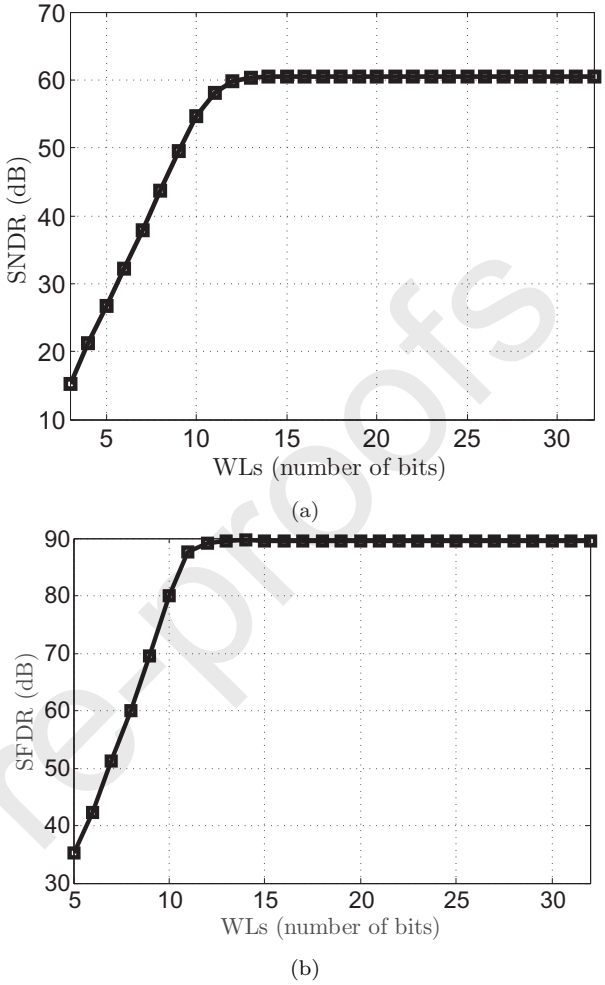


Fig. 13: SNDR/SFDR vs. WLs of the compensated TIADC output: (a) SNDR. (b) SFDR.

and also allows access to real hardware in the simulation environment. The implementation results demonstrate that the synthesized circuit operates properly on the FPGA hardware platform and consumes very small amount of hardware resources of the FPGA chip (Kintex-7 XC7K325T device) as shown in Table 2.

Table 2: FPGA implementation results.

Family	Xilinx Kintex-7
Device	XC7K325T
Logic cells utilization	6,777/203,800 (3.33%)
Distributed LUT RAM	177/64,000 (0.28%)
Flip-Flops (FFs)	6,053/407,600 (1.49%)
DSP slices	19/840 (2.26%)
Fmax	165.7MHz

Table 3 presents the performance comparison of the synthesized digital logic in FPGA implementation using FIL methodology with the state-of-the-art techniques. The proposed calibration technique is completely blind and uses the ANC technique that effectively estimates the gain and clock skew errors. It keeps gain and clock skew tones at -87 dB and provides high convergence speed demonstrating the good performance of our proposed approach.

5 Conclusion

In this paper, a novel ANC-based all-digital blind background calibration technique of the gain and timing mismatches in TIADCs has been proposed. By producing the linear presentation of the distortion signals, the gain and clock skew mismatch coefficients are esti-

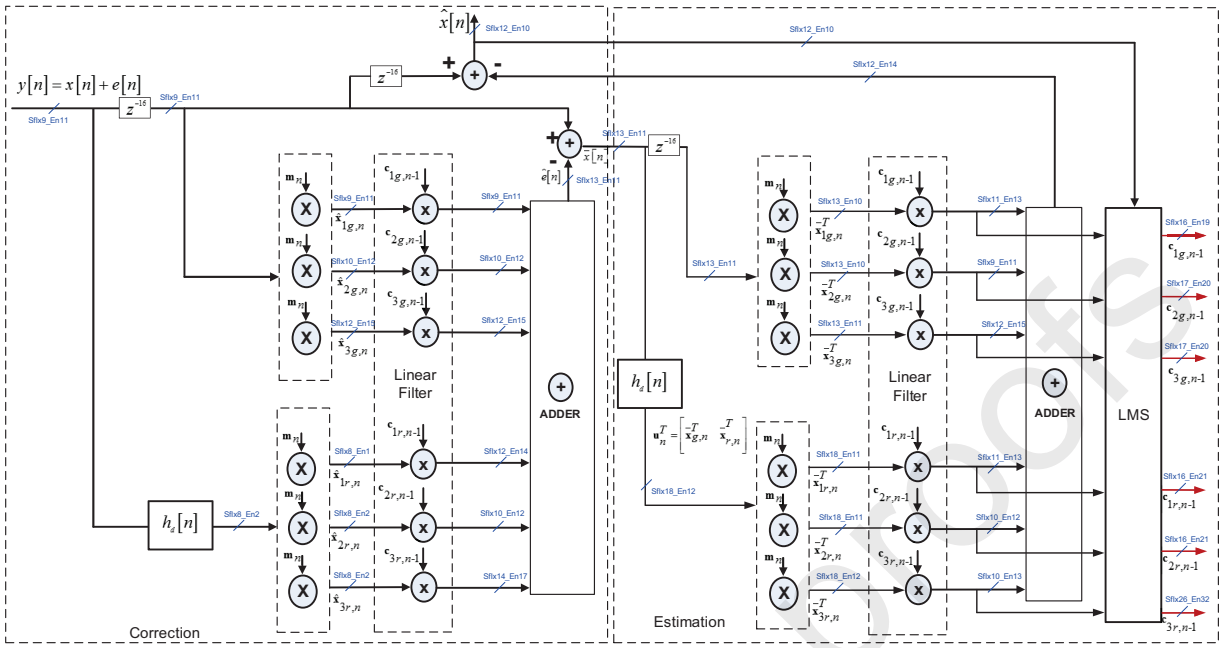


Fig. 14: The optimal fixed-point hardware architecture of the proposed calibration.

Table 3: Comparison of implementation results with the state-of-the-art techniques.

	This Work	[19] VLSI-2017	[12] TCAS-I 2013	[5] TCAS-I 2017	[18] ICECS 2008	[22] ISSCC 2014
Number of bits	11	12	10	11	–	12
Sample frequency	2.7 GHz	2 GHz	–	2.7 GHz	–	1.62 GHz
Number of channel	4	4	2	4	4	12
Blind	**Blind**	Blind	Blind	Blind	Semi-blind	Blind
Derivative generation	**FIR filter**	FIR filter	FIR filter	Polyphase FIR filter	FIR filter	FIR filter
Gain/timing error estimation	**ANC**	Subtraction detection	FIR filter +correlator	Open-loop calculator	Free-band estimation	Subtraction detection
Mismatch tone level	−87 dB$^{(*)}$	−62 dB	−80 dB	−97 dB	−60 dB	−78 dB
Convergence time (Samples)	20 K	80 K	60 K	10 K	80 K	1 M

(*) for the synthesized logic circuit of the proposed calibration in FIL methodology at input frequency of 1.134MHz.

mated when the output SNR of ANC systems is maximized. In correction, the error signals are reconstructed and then subtracted from the distorted TIADC output to achieve the compensated signals. The proposed technique releases the input spectrum constraints and does not require high-pass filters, hence reduces the hardware cost. In other words, it overcomes the limitation of the conventional free-band based calibration technique. The implementation results including FPGA validation have confirmed that the gain and timing distortions can be almost fully compensated by employing the ANC based calibration in the 11-bit, 4-channel TIADC clocked at 2.7GHz for various input signals. The proposed calibration shows its good performance in terms of SNDR and SFDR improvement of 19 dB and 49 dB, respectively. It is also validated on an FPGA hardware

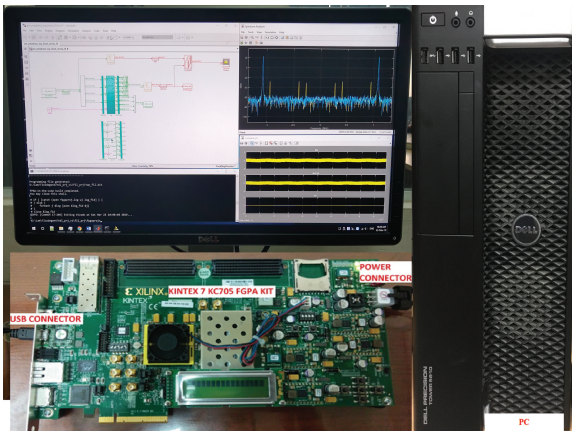


Fig. 15: Experimental platform for FPGA implementation.

platform with the Xilinx Kintex-7 board. The synthesized digital circuit costs only 7.36% of the hardware resources of the FPGA chip and keeps the mismatch tone level at −87 dB. In the future work, we will carry out the application specific integrated circuit (ASIC) implementation of the proposed calibration technique in order to estimate the detail chip area and power consumption.

Acknowledgment

This research is funded by Vietnam National Foundation for Science and Technology Development (NAFOSTED) under grant number 102.02-2016.12.

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