An Adaptive Continuous-Time Linear Equalizer Using Sampled Data Edge Counting

Pham Manh Ha, Nguyen Huu Tho, and Quang-Nguyen The
Dept. of Communication Engineering, Le Quy Don Technical University
236 Hoang Quoc Viet, Co Nhue, Bac Tu Liem, Ha Noi, Viet Nam
E-mail: tho.nh@mta.edu.vn, quangnt@mta.edu.vn

***Abstract*— In this paper, an adaptive continuous-time linear Equalizer (CTLE) utilizing a proposed sampled data edge counting for multi Gb/s serial links is presented. The compensation level of the equalizer is determined by counting and comparing rising edges the sampled data and fed back to the CTLE. The proposed algorithm is verified with a High-Definition Multimedia Interface (HDMI) 2.0 cable at 3 Gb/s data rate using a 180 nm CMOS process technology. The simulation shows the adaptive EQ achieves compensation range from 3 dB to 24.8 dB with a tuning range of 21.8 dB and adaptation time of 4.6 µs.**

***Keywords*— optical communication, high speed interface, continuous time linear equalizer, adaptive equalizer**

I. INTRODUCTION

In high-speed wireline communication systems, inter-symbol interference (ISI) due to frequency-dependent channel losses becomes a serious issue. To counteract the effects of the communication channel, equalization is widely used in various types. In addition, the characteristics of the communication channel are not always known prior to transmission. For this reason, it is strongly desired to have adaptive equalization. In this case, the receiver adapts the equalizer to compensate losses for different channel conditions. Various adaptive equalizers have been presented [1]-[9]. They are divided into three main methods. The first one uses filters: low-pass, high-pass, or all-pass [1]-[5]. In [1], [2], [5], the adaptive equalization obtained by comparing the power of the high and low frequency components of data. In [3], a slope detector is used to compare slope of data before and after a limiter to adjust the equalizer. In [4], both peak detection and power detection technique are used to archive both optimum low-frequency gain and optimum high-frequency boost. However, their implementation requires complicated analog circuits. Moreover, performance of power detector, slope detector and peak detector can be sensitive to the process variation. The second one is a promising adaptive equalization technique in which uses an eye-opening monitor (EOM) [6], [7]. The basic adaptive equalization principle of this method based on desired bit error ratio (BER), but in reference [6], equalization cannot realize with initially closed eye diagram lead to limit its applicability. In reference [7], the equalization performance strongly depends to the input data density. The last one performs adaptive equalization by using counter [8], [9]. In [8], a large amount of data is asynchronously sampled to have the data histograms which are used to adjust the equalizer. However, the huge digital memory circuits are needed and the adaptation time is long. In reference [9], a data edge counting technique is shown to adaptively adjust the gain of the equalizer.

Instead of data edge counting, we propose counting the sampled data edge. Whereas the number of sampled data edges is much more sensitive to the ISI than the number of data edges itself, this proposal presents a higher distinguishable for finding the optimal value in the adaptive equalization.

The remainder of this paper is organized as follows. The architecture of the equalizer, adaptive algorithm and detailed descriptions of the sub-blocks are described in Section II. Section III provides the experimental results on 180 nm CMOS process followed by conclusions in Section IV.

II. CIRCUIT DESCRIPTION

Our adaptive equalization algorithm is based on a simple principle that the number of sampled data edges is larger when the ISI effect is small and vice versa. Fig.1 shows comparison between work in [9] and this proposal, and its timing diagram is shown in Fig.2 with the ISI-induced. Obviously, with missing of some values N2 because of the ISI, the sampled data edge counting is more sensitive to the ISI than the data edge counting. On the other hand, this proposal works more accurate than [9].

The diagram of adaptive continuous-time linear equalizer (CTLE) is shown in Fig. 3, which includes the CTLE, a CML/CMOS converter, a D-type flip-flop (D-FF), an 8-bit counter, a data latch, a comparator, a digital controller, a voltage control oscillator (VCO) and a clock divider.

2.1. Adaptive equalization algorithm

Fig.4 presents the adaptive equalization algorithm for the proposed equalizer. The adaptation process is divided into two periods. In the first period, the high-frequency gain of the CTLE is established maximal, i.e., C[3:0] = 1111. The equalized data passes the CML/CMOS converter, after that is sampled at the D-FF by a synchronous clock from the clock

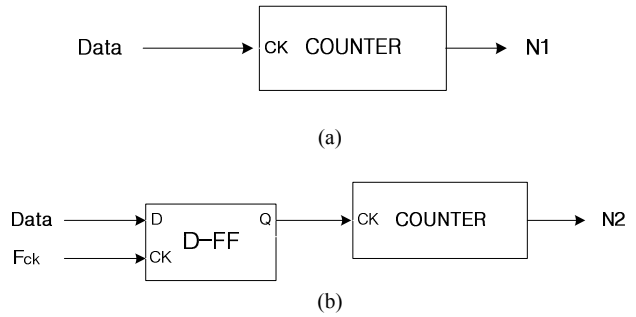

Fig. 1. (a) Block diagram of work in [9], (b) block diagram of present work

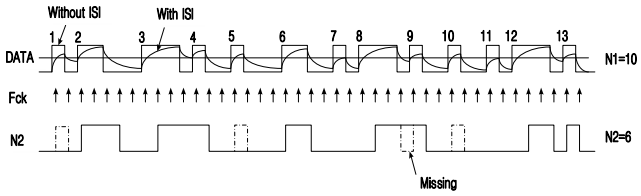

Fig. 2. Timing diagram of the Fig.1

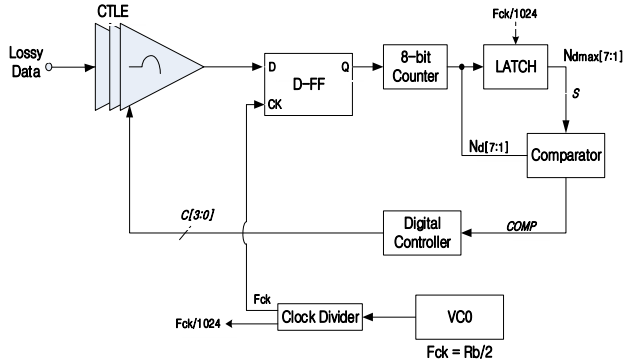

Fig. 3. Block diagram of proposed adaptive equalizer

divider, i.e., F_{ck} = R_b/2, then the sampled data edges are counted by the 8-bit counter, the result is stored in Latch circuit as N_{dmax}[7:0]. The Latch circuit only works one time in initial state. After getting value N_{dmax}[7:0], the high-frequency gain of the CTLE is reset to minimal, i.e., C[3:0] = 0000, the second period of adaptation process starts. The value N_d[7:1] which gets from the 8-bit counter is compared to N_{dmax}[7:1] that is stored in the first period of the adaptation process. If N_d[7:1] is less than N_{dmax}[7:1], the signal *COMP* will be low and the digital controller increases the code C[3:0] to raise the high-frequency gain of the CTLE. When N_d[7:1] is equal or more than N_{dmax}[7:1], the signal *COMP* goes high. The code C[3:0] is fixed, the equalizer finds optimal high-frequency gain and adaptation process is completed.

2.2. Operation of Latch and Comparator circuit

The timing diagram of latch and comparison operation is shown in Fig. 5. The clock divider generates two clocks, the first one, i.e., F_{ck} = R_b/2, samples the input data and the second one, i.e., F_{ck}/1024, creates a timing window of 512T_{ck} in count mode. In this mode, the signal *S* will arise at 432T_{ck}. The

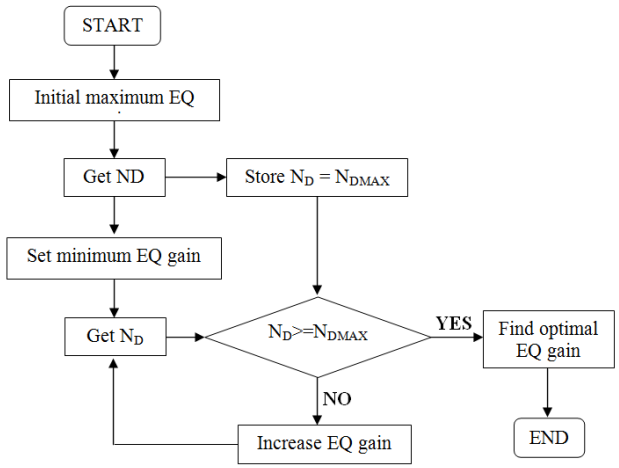

Fig. 4. Adaptive equalization algorithm

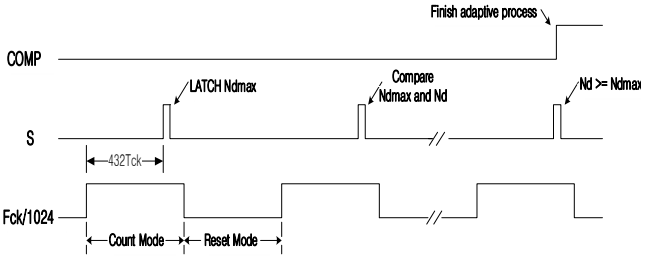

Fig. 5. Operation of Latch and Comparator

N_d[7:0] is stored as N_{dmax}[7:0] when the signal *S* arises in the first time, in the next times, the N_d[7:1] is compared to N_{dmax}[7:1] to adapt equalizer. When N_d[7:1] is equal or more than N_{dmax}[7:1], the signal *COMP* goes high to finish adaptive equalization.

2.3. Continuous-Time Linear Equalizer (CTLE)

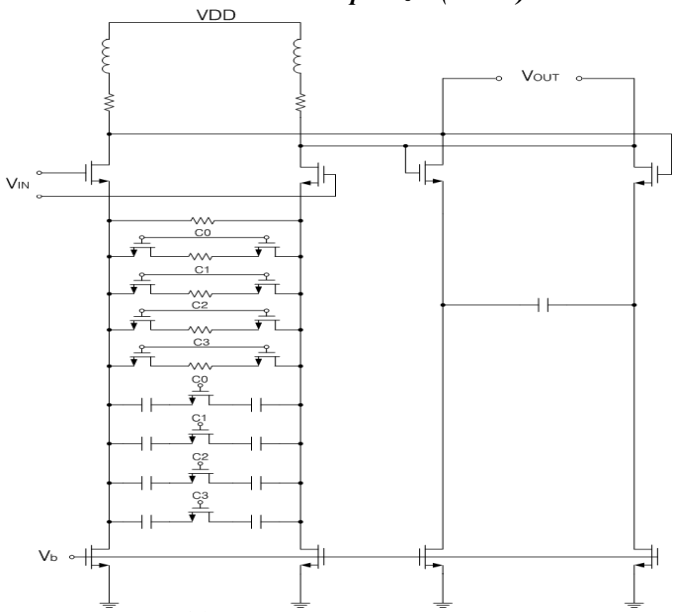

Fig. 6. One stage of the CTLE circuit

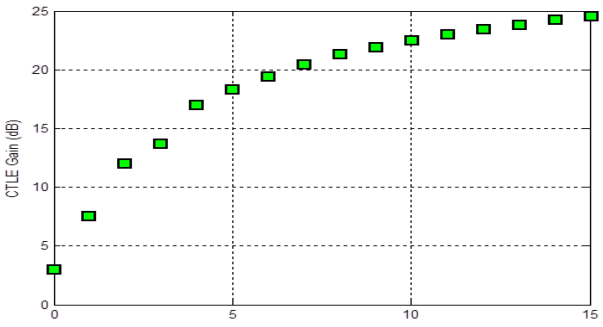

Fig. 7. Gain boosting of the CTLE

To achieve channel loss compensation of -16.5 dB at 3Gbps, we design three-stage capacitive degeneration filter as shown in Fig. 6. The gain stage uses the inductive peaking and negative capacitor [3] technique to enhance the bandwidth. The 4-bit NMOS resistor and capacitor array provide 16 different levels of gain boosting for the CTLE as shown in Fig. 7.

III. SIMULATION RESULTS

The proposed adaptive equalizer is implemented in a 180 nm CMOS process. The simulation results show that the proposed EQ circuit works well with a given channel. Adaptive circuit obtains adaptation time of 4.6 µs. The CTLE gain code is adaptively determined by circuit without any external control.

To demonstrate tracking ability of the proposed adaptive algorithm operation, we use an equivalent channel model of High-Definition Multimedia Interface (HDMI) 2.0 cable with channel loss of -16.5 dB at 3 Gb/s as shown in Fig. 8. Fig. 9 shows the latch operation, adaptation of the EQ. At the first time, the CTLE gain code C[3:0] is set equal to 1111 to maximum the high-frequency gain of the CTLE. During this time, the output of 8-bit counter B[7:0] is stored as D[7:0]. After that, the C[3:0] is reset equal to 0000 to minimum the high-frequency gain of the CTLE and start the adaptation process. The CTLE gain code C[3:0] is adapted by comparing between B[7:1] and D[7:1]. When B[7:1] is equal or more than D[7:1], adaptation algorithm finishes. The adaptive EQ locks at the CTLE gain code of 0010 and the CTLE boosting gain of 16.8 dB.

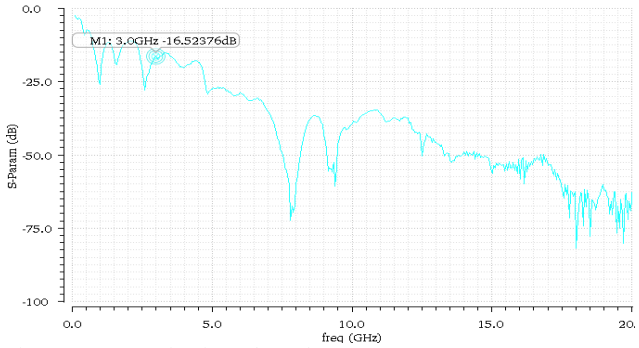

Fig. 8. Response of a given channel

A simulation for both the work in [9] and this proposal is implemented with same condition to verify efficiency of this work. Table I shows comparison of EQs about accuracy. In which the second column is data before equalization, the third column is data after equalization of work in [9], and the last column is data after equalization of this proposal; dX is eye-open in horizontal of data eye-diagram, dY is eye-open in vertical of data eye-diagram. This work obtains a wider eye-open than previous work in both vertical and horizontal axes (230 ns in time and 772 mV in voltage). Consequence, by counting sampled data edges instead of data edges, the proposed adaptive EQ works well than the EQ in [9].

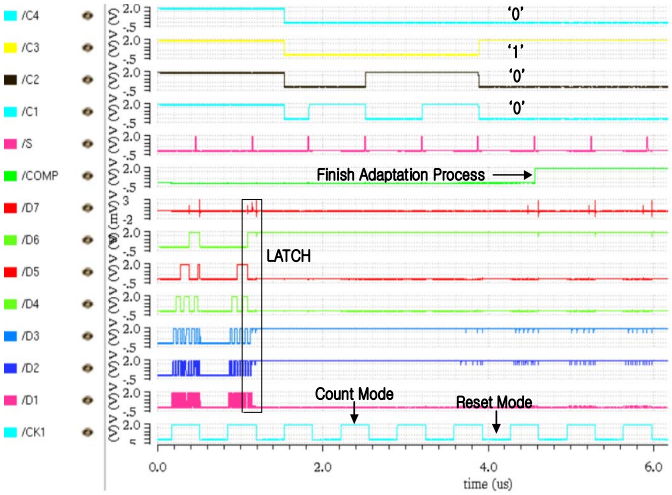

Fig. 9. Simulation result of the adaptive Equalizer at 3Gbps

Table I. Comparison about adaptive efficiency of EQ in [9] and this proposal

	Before Equalization	**[9]**	**This paper**
dX (ns)	216	185	230
dY (mV)	102	739	772
CTLE boosting gain (dB)		12	16.8
CTLE gain code C[3:0]		0010	0100

IV. CONCLUSION

An adaptive continuous-time linear equalizer with counting the sampled data edges is presented. The proposed equalizer obtains high sensitive with the ISI and less sensitive to variation of voltage, process and temparature. The proposed adaptive algorithm is verified with a HDMI 2.0 cable of −16.5 dB attenuation at 3 Gb/s data rate. The proposed adaptive equalizer compensates from 3 dB to 24.8 dB, 21.8 dB of tuning range with 16 different levels. The adaptation time of the proposed architecture is 4.6 µs using a 180 nm CMOS process technology.

REFERENCES

[1] J.Lee, et al., "A 20-Gbs Adaptive Equalizer in 0.13um CMOS Technology," *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 41, no. 9, SEP. 2006.

[2] K.H.Cheng, et. al., "A 5-Gbs Inductorless CMOS Adaptive Equalizer for PCI Express Generation II Applications," *IEEE TRANSACTIONS ON CIRCUIT AND SYSTEMS-I,* vol. 57, no. 5, MAY. 2010.

[3] D.Lee, et al., "An 8.5 Gbs Fully Integrated CMOS Optoelectronic Receiver Using Slope Detection Adaptive Equalizer," *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 45, no. 12, DEC. 2010.

[4] H.Liu, et al., "A 5-Gbs Serial-Link Redriver With Adaptive Equalizer and Transmitter Swing Enhancement," *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I*, vol. 61, no. 4, APRIL 2014.

[5] B.Nakhkoob, and M.Hella, "A 4.7Gbs Reconfigurable CMOS Imaging Optical Receiver Utilizing Adaptive Spectrum Balancing Equalizer," *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I*, vol. 64, no. 1, JAN. 2017.

[6] S. Son, et al., "A 2.3-mW, 5-Gb/s low-power decision-feedback equalizer receiver front-end and its two-step, minimum bit-error-rate adaptation algorithm," *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 48, no. 11, pp. 2693–2704, Nov. 2013.

[7] H.Won, et al., "A 28-Gbs Receiver With Self-contained Adaptive Equalization and Sampling Point Control Using Stochastic Sigma-Tracking Eye-Opening Monitor," TCAS-I, vol. 64, March, 2017.

[8] W.S.Kim, et al., "A 5.4Gb/s adaptive equalizer using asynchronous sampling histograms," *in ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 358–359.

[9] Y.-F. Lin et al., "A 5–20 Gb/s power scalable adaptive linear equalizer using edge counting," *in Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2014, pp. 273–276.