A Wide-band Reference-less Bidirectional Continuous-Rate Frequency Detector

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Abstract— This paper presents a wide-band half-rate frequency locked loop (FLL) circuit in 180 nm CMOS process. The bidirectional FLL includes a coarse frequency detector (CFD) and a fine frequency detector (FFD) to automatically detect a change in input data rate, acquires the new frequency without the need for an external reference clock or any programming. A modified CFD is proposed to reduce the frequency acquisition time. The simulation shows the FLL achieves wide lock range of 400Mb/s-to-2.6Gb/s and frequency acquisition time of 1.73 µs.

Keywords— *Bidirectional frequency detector, reference-less, wide-band, continuous-rate, clock and data recovery*

I. INTRODUCTION

The frequency detector (FD) plays a very important role in reference-less clock and data recovery (CDR) circuits to extend frequency acquisition range of the CDR. So far, we have had several methods of frequency detection in the reference-less CDR. The first one is quadricorrelator frequency detectors (QFDs) [1, 2, 3]. In this method, FDs use quadrature clocks to sample the input data or vice versa to determine the frequency error without an external reference. Although the modified digital QFD (MDQFD) can remove jitter effect, and the DQFD can track bidirectional frequency the DQFD has limited locking range of ± 25% in [2, 3] and ± 13 % in [1]. The second method is a delay-locked loop (DLL)-based frequency acquisition [4]. A wide-range reference-less continuous-rate FD is achieved by combining the coarse/fine delay acquisition scheme. However, in this approach the initial delay of voltage controlled delay line (VCDL) is set to be the minimum. In other words, the voltage controlled oscillator (VCO) always resets to its maximum frequency for a new acquisition process. That means frequency acquisition time could be longer. Moreover, any mismatching between a VCDL and a VCO will cause more jitter in recovery clock and data at the CDR output. The third one is a stochastic reference clock generator (SRCG)-based frequency acquisition technique [6]-[8] in which a clocklike periodic signal is generated from a random non-return-to-zero data sequence to extract frequency error. This approach consumes low power while simultaneously achieving bidirectional frequency tracking. However, this method generates a very low frequency for the reference frequency that means it requires a long frequency acquisition process. In addition, it also assumes a pre-defined input data transition density for frequency tracking. Any the frequency offset between the acquired clocklike signal and the ideal clock signal degrades the CDR performance. In other words, accuracy of the FD in

reference [6] strongly depends on the input data transition density, so it is not suitable for the CDRs in which have various transition density of the input data. The fourth one is a phase detector (PD)-based frequency acquisition technique [9]-[13] where they use intrinsic frequency detection capability of bang-bang PD or linear PD, or they modify some part of or add some special function blocks to the PD to detect frequency difference. Although reference [9]-[13] do not rely neither on a separate frequency detector nor an external reference clock, they suffer some disadvantages. Reference [9], [11], [12] only have a narrow lock range with 20%, 21%, and 36%, respectively, so they are not suitable for applications that require a wide-range of the input data rate. Reference [10], [13] obtain a wider lock range, but it is not a continuous-rate CDR [13], and a reference frequency is used to implement a digitally controlled oscillator lead to the CDR is not full reference-less [10]. Moreover, reference [10], [11], [13] have architecture of a unilateral FD. They realize a linear search so that searching algorithms scan whole frequency range from the minimum [10], [13] or maximum [11] until they find out the target, hence increasing frequency acquisition time. The last one is counting-based frequency acquisition technique [5], [14], [15]. This approach achieves a wide frequency acquisition and a bidirectional FD, but [5] and [15] are not a continuous-rate FD, the FD strongly depends on the inter-symbol interference (ISI)-induced of the input data [14]. This paper proposes a simple wide-band bidirectional reference-less continuous-rate FLL combining a coarse-FD and a fine-FD in which could applies in reference-less CDR circuits.

The remainder of this paper is organized as follows. The overall FLL architecture with concept of the proposed FD scheme and circuit implementation are described in detail in Section II. Section III presents the experimental results on 180 nm CMOS process. Finally, the conclusions are provided in Section IV.
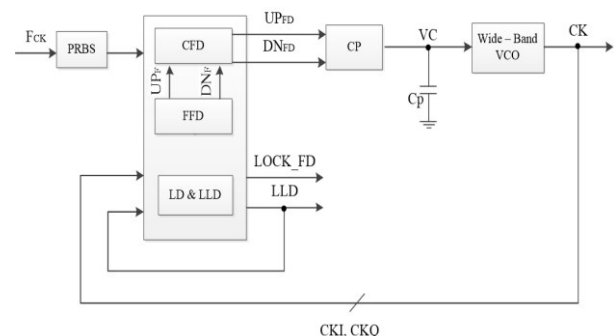

Fig.1. The block diagram of the proposed FLL.

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II. CIRCUIT DESCRIPTION

The block diagram of the proposed half-rate reference-less frequency locked loop (FLL) circuit is shown in Fig. 1. It includes a modified coarse frequency detector (CFD), a modified fine frequency detector (FFD), a frequency lock detector (LD), a loss of lock detector (LoLD), a wide-band VCO [15], a capacitor, and a charge pump (CP) circuits.

In Fig. 1, a clock signal is entered a Pseudorandom binary sequence (PRBS) block to generate input data for the FLL. The proposed FD tracks the frequency error between the input data and the output clocks, i.e., CKI and CKQ. Once the frequency error is small enough, a LOCK_FD signal is triggered by the LD to finish frequency tracking process. After that, the LoLD starts to operate. When the LoLD detect a variation of the input data rate, it generates a LLD signal to reset the FLL, starts a new frequency acquisition process simultaneously.

A. Proposed CFD

Fig. 2 shows the proposed CFD. This proposed CFD consists of a frequency increment acquisition FD, a frequency decrement acquisition FD, a D-type flip-flop (D-FF), two OR-gate, and two multiplexers. In which, the signal UP_F and DN_F at the OR-gate input come from the output FFD, the signal UP_{FD}, DN_{FD} is given the CP to charge/ discharge the loop filter to increase/ decrease the clock frequency, respectively.

When the signal UP_C, the output of the frequency increment acquisition CFD, arises, the signal STOP is generated at the output of a positive-edge-triggered D-FF. The signal STOP is used to control selection UP_C/DN_C signal at the output of the CFD. The operation principle of the proposed CFD is presented specifically as follows:

① STOP = 0:
- $UP_{FD} = UP_{coarse} = UP_C$
- $DN_{FD} = DN_{coarse} + DN_{fine} = DN_C + DN_F$
② STOP = 1:
- $UP_{FD} = UP_{coarse} + UP_{fine} = UP_C + UP_F$
- $DN_{FD} = DN_{fine} = DN_F$
when the FD closes to frequency locked state, $UP_C \approx 0$, thus
$$UP_{FD} \approx UP_{fine} = UP_F$$

As a result, the proposed architecture of the CFD allows the CFD and the FFD to operate simultaneously. When the CDR closes to frequency locked state, the CFD stops working automatically. The FD remains the FFD in operation. In another word, no exist pulse UP_C and DN_C
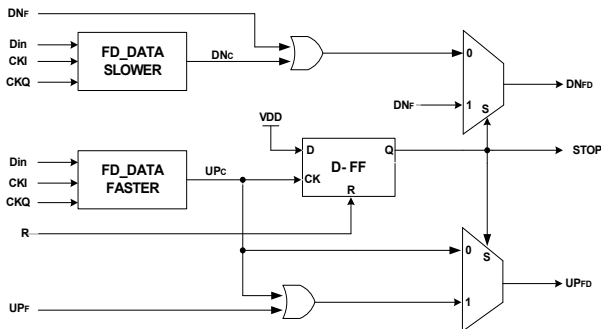
Fig. 2. The block diagram of the proposed CFD.

at the output of the CFD. Therefore, this architecture eliminates needfulness an additional CP, increases probability in which the pulse UP_{FD} and DN_{FD} appear as well.

The bidirectional FD has the advantage of short frequency acquisition time. The CDR can track the input data rate at any value of the VCO frequency in its operation range (not compulsoriness at minimum or maximum frequency of the VCO). The reference [15] presented a simple frequency tracking method by counting the number of consecutive transition edges of the clock in sequence "010" and "011"of the data for frequency decrement acquisition to remove necessary of quadrature divider in [5]. In addition, in [15] the frequency increment acquisition used two phases of clock, i.e., CKI and CKQ instead of one phase of clock [5], and detected both specific patterns "101" and "010" of the data instead of one specific pattern [5] to
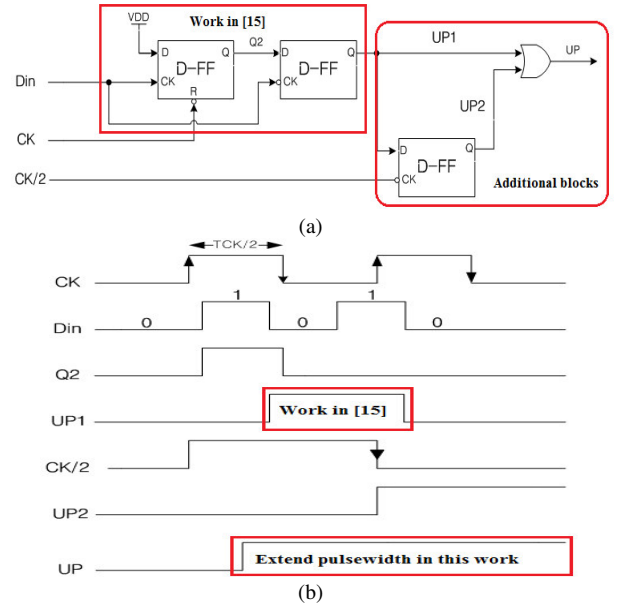
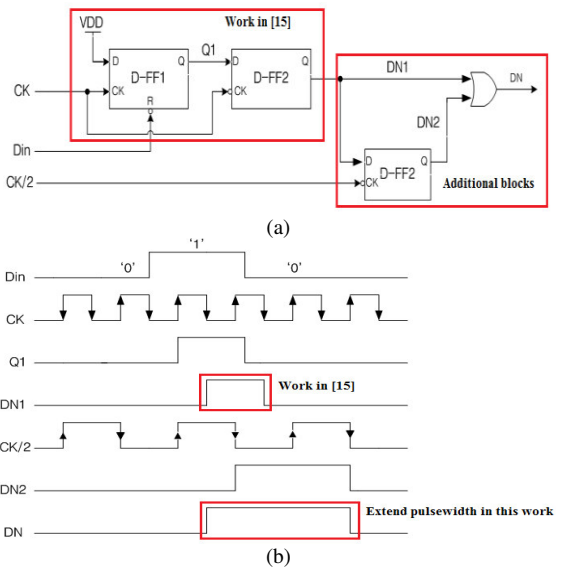Fig. 3. (a) The block diagram of the frequency increment acquisition CFD, (b) It's timing diagram.

Fig. 4. (a) The block diagram of the frequency decrement acquisition CFD, (b) It's timing diagram.

TABLE I. Comparison of FDs about the VCO frequency change rate

	Slew rate (SR) [mV/us]
Frequency increment acquisition FD in [15]	16.5
Frequency decrement acquisition FD in [15]	29.5
New frequency increment acquisition CFD	30.2
New frequency decrement acquisition CFD	84.4

reduce frequency acquisition time. However, the pulsewidth UP and DN at the output FD in [15] are relatively small, so in this paper, we propose additional some simple blocks into the bidirectional FD to extend the pulsewidth UP and DN at the output FD.

The unilateral CFD that detects whether the data rate is faster than the clock is shown in Fig. 3(a) and its timing diagram is shown in Fig. 3(b). Only a D-FF and an OR-gate are added into the frequency increment acquisition circuit, hence no more additional power and area. The output FD in [6] is sampled by a half the phase of clock using a negative-edge-triggered D-FF. The final signal UP is created by combining the output from the FD (UP1) and the output from the D-FF2 (UP2) at the OR-gate.

The unilateral CFD that detects whether the data rate is slower than the clock is shown in Fig. 4(a) and its timing diagram is shown in Fig. 4(b). The same method as the frequency increment acquisition CFD, a D-FF and an OR-gate are added to extend the pulsewidth of the signal DN.

To verify efficiency of this proposal, a simulation for both the work in [15] and this modification is implemented with the same condition.

The Table I shows comparison of FDs about the VCO frequency change rate. The VCO frequency change rate of the proposed CFD is approximately more than double the work in [15]. Obviously, with wider pulsewidth of the signal UP and DN, the new CFD archives shorter frequency acquisition time.

B. Proposed FFD

In this work, we propose a simple circuit modifying DQFD (M-DQFD) [1], where only uses two clock phases. The reference [1] presents a frequency detection method for half-rate CDR, digital quadricorrelator frequency detector (DQFD). However, the frequency detector requires four clock phases. In generation, buffering, and sampling with multiple phases of clock introduce power and area overhead. The block diagram and its timing diagram of the proposed FFD are shown in Fig.5.

Four D-FFs triggered by data are used to store the sampled values and record the states, as shown in Fig. 5(a). In the proposed M-DQFD, each clock period is divided into four states, 1, 2, 3, and 4, as shown in Fig. 5(b). Suppose that the first rising edge of data appears at the boundary between state 1 and state 2. Then, if the second rising edge appears at the boundary between state 4 and state 1. The state transition rotated from state 4 to state 1 would be detected. This state transition would indicate that the data rate is faster than the clock frequency; i.e., the signal UP will be active. In another case, if the second rising edge of data arises at the boundary between state 2 and state 3. The
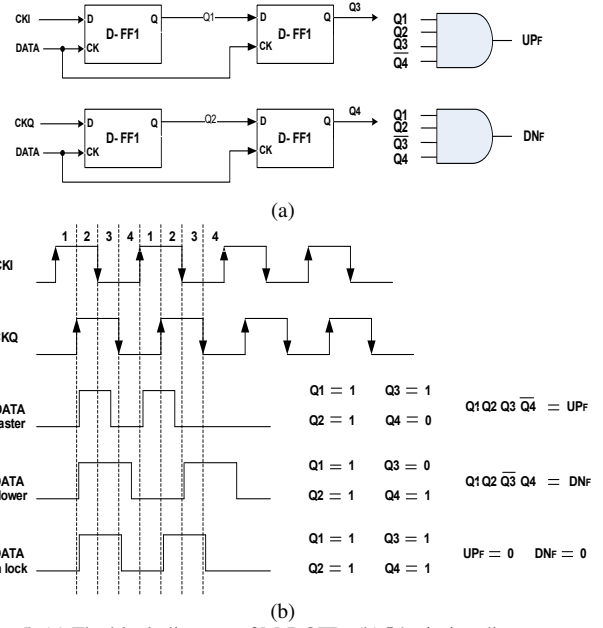

(a)

(b)

Fig. 5. (a) The block diagram of M-DQFD, (b) It's timing diagram
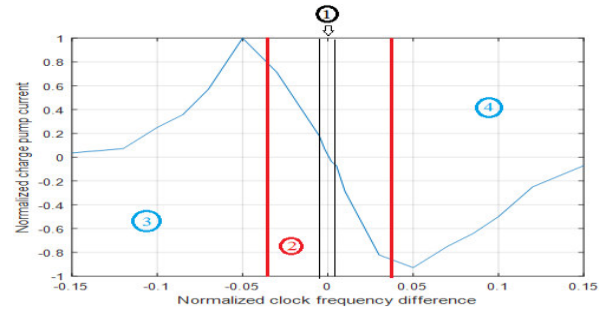

Fig. 6. Transfer curve of the M-DQFD.

state transition rotated from state 2 to state 3 would be detected. This state transition would indicate that the data rate is slower than the clock frequency; i.e., the signal DN will be active. In locked condition, both the first rising edge and the second rising edge of data appear at the boundary between state 1 and state 2. Consequently, no pulse UP or DN would be active.

C. Lock Detector/ Loss of Lock Detector

The LD and LoLD circuits monitor the output from the FFD to decide that the FD is in lock or loss of lock.

The transfer curve of the M-DQFD is divided into four regions as Fig.6. Where region 1 is region which the CDR is in frequency lock state. The region 2 reveals that the frequency error increases but relatively small. When the FLL start a frequency acquisition process, the frequency error is large and is shown in region 3 and 4. At this time, the CFD and the FFD operate together. As a result, the frequency error decreases. According to property of the M-DQFD, when the frequency error is small enough (in region 1) the LD triggers a signal LOCK to indicate that the FD is in lock state. Then, the LoLD starts monitoring the variable input data rate. If the LoLD realize a variation of the data rate that causes an increasing frequency error (transition from region 1 to region 2), it will trigger a signal LLD to reset the FLL into a new frequency acquisition process.

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III. SIMULATION RESULT

To verify working ability of the proposed FLL with continuous-rate of input data, a simulation model is shown in Fig. 7 which consists of two PRBS blocks to generate various data rate, a MUX block with selected signal *S* to select data, and the proposed FLL with output data of *VC, LOCK_FD, LLD, F_{CK}* for checking.

The proposed FLL circuit is implemented in a 180 nm CMOS process. The simulation results in Fig. 8 show that the circuit successfully tracks frequency with PRBS7 pattern. The operating data rate range of the proposed FD is unlimited. It can be extended by increasing the frequency range of the VCO. Fig. 8 shows two periods of frequency acquisition responses when the initial frequency of the VCO is 400MHz. The first period responds to data rate of 2Gbps. When the VCO frequency closes to 1GHz, the signal *LOCK_FD* is trigged to complete frequency tracking process. The FLL is in locked state. After that, the signal *S* is switched from '0' to '1' to change data rate from 2Gbps to 1.5Gbps. The LLD observes this variation, it generates the signal LLD to reset the FLL circuit. The FLL starts a new frequency acquisition process and obtains again locked state. The technical comparisons with other FLLs are shown in Table II.

IV. CONCLUSION

A reference-less wide-band FLL circuit is implemented in 180nm CMOS process. The proposed bidirectional FD is free from harmonic locking issue, does not depend on run-length and density of the input data. It eliminates the depending of the input data rate as well. In additional, the proposed FD achieves an unlimited frequency acquisition range. It has the short frequency acquisition time of 0.38 µs and 1.73 µs in simulation for the decrement acquisition and increment acquisition, respectively, with average power consumption of 23.94 mW at 2 Gb/s.
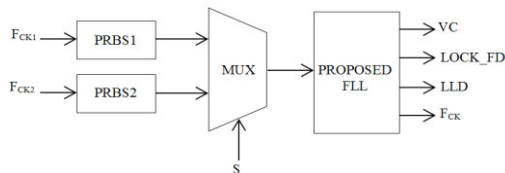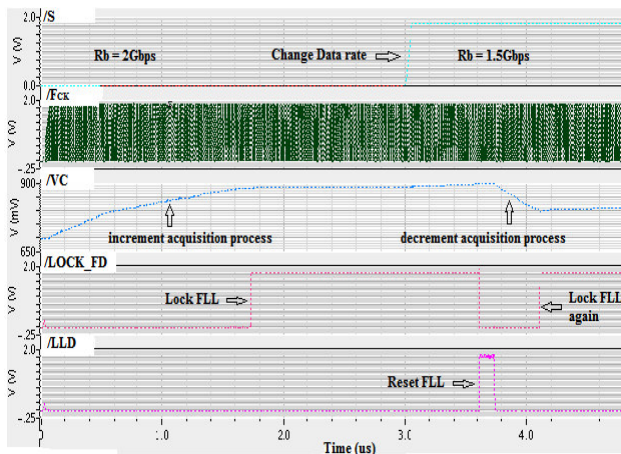

Fig. 7. Simulation model for the proposed FLL.

Fig. 8. Simulation result of the proposed FLL

TABLE II. TECHNICAL COMPARISION OF WIDE-BAND REFERENCE-LESS FLL

	[5]	[14]	[15]	This work
Technology (nm)	130 CMOS	65 CMOS	180 CMOS	180 CMOS
Supply (V)	1.5	1	1.8	1.8
Continuous-data rate	No	Yes	No	Yes
Freq.acquisition time (µs)	1000	52	12.9	1.73
Sensitiveness with input data transition density	No	Yes	No	No
Power (mW)	160 (CDR) @10Gb/s	18.7 (CDR) @10Gb/s	37.8 (CDR) @3Gb/s	23.94 (FLL) @2Gb/s

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