Design and Implementation of Signal Processing Unit for Two-Way Relay Node in MIMO-SDM-PNC System

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***Abstract*—This paper investigates design and implementation of the signal processing unit for the relay node in a two-way relay multiple-input multiple-output spatial division multiplexing (MIMO-SDM) system using physical-layer network coding (PNC), reffered to as MIMO-SDM-PNC. Based on Field-programmable gate array (FPGA) platform, two processing architectures for zero-forcing (ZF) and minimum mean square error (MMSE) detector are proposed for the relay node. Using the standard pipe-lining and the parallel computing methodologies, a novel architecture is developed in order to achieve low latency and low-area occupation for FPGA implementation. The proposed architecture has been composed in Verilog language and synthesized on the ISE tool for Xilinx FPGA Virtex 7. Experimental results demonstrate that the proposed design offers high performance in terms of low latency and high throughput.**

***Index Terms*—MIMO, SDM, PNC, DSP, ZF, MMSE, FPGA**

I. Introduction

In order to enhance capacity and coverage of cellular communication systems, wireless relaying has been considered a promising scheme and included in recent broadband radio standards [1]. Recent researches also showed that relay communications can achieve significant improvement in providing quality of service (QoS) and system performance, reducing outage probability and transmission power [2], [3]. However, conventional relaying schemes reduce bandwidth efficiency, system throughput and capacity as it requires multiple time slots for bidirectional data exchange. There have been significant efforts in striving to overcome these problems [4]–[7] among which network coding (NC) appears as a potential solution [8]–[10].

In the conventional two-hop bi-directional communication networks NC can be applied to reduce the required number of time slots from four to three using appropriate symbol encoding at the relay. Further implementation of NC at the physical layer, which results in the physical-layer NC (PNC), can save one more time slot [11]. In paper [11], Zhang *et al.* demonstrated that throughput of the PNC system can increase by 200% and 150% in comparison with the non-NC and the NC system, respectively.

Recently, PNC was also introduced in the two-way relay multiple-input multiple-output (MIMO) system [12]. In the MIMO-PNC system, the network-coded symbols at the relay are created using the summation and difference components from the two terminal nodes. The MIMO-PNC scheme does not require strict synchronization for the carrier phase while producing higher performance than that in the conventional MIMO-NC schemes in the case of Rayleigh fading. In paper [13], the authors proposed the channel coding and physical-layer network coding (CPNC) for a two-way relay MIMO system. The proposed method converts the received streams from two sources to the relay node into parallel streams, leading to a capacity achievement close to an upper theoretical bound. Furthermore, Zhang *et al.* proposed the Vertical-Bell Laboratories Layered Space-Time (V-BLAST)-PNC scheme that superimposes the received packets at the relay node into a network coding form, which can use the V-BLAST algorithm to estimate the summation and difference versions of the received signals from two sources. In addition, the space-division multiplexed (SDM)-PNC for the MIMO channel was proposed in [14]. The proposed MIMO-SDM-PNC system has the same diversity order, however, attains double multiplexing gain compared with the MIMO-PNC system while it does not require channel state information (CSI) of the links from two source nodes to the relay node. In this paper, we focus our attention on design and implementation of the signal processing unit at the relay node in a bidirectional MIMO-SDM-PNC system.

The challenge in the signal processing for MIMO systems is to ensure high computing performance, to implement computationally intensive operations and to achieve low latency while all calculations need to be reliable. With the above requirements, computation and processing for MIMO systems can be implemented on FPGA and ASIC platforms. There were also several researches on implementation of MIMO systems in the literature. For instance, Dowle *et al.* developed a space-time array research (STAR) platform for a MIMO system which requires less effort and results in a more stable system than a similar digital signal processing (DSP) one implemented in [15]. An implementation of STBC systems was introduced and presented in [16]. In [17], [18], an FPGA-based architecture for both sphere decoder (SD) and fixed

sphere decoder (FSD) was proposed for MIMO systems. In addition, the encoder for an Alamouti STBC system with two transmit and four receive antennas was designed and implemented in [19] while an implementation of the decoder for MIMO systems was developed in [20]. In paper [21], an FPGA architecture for the sorted QR decomposition (SQRD) detector at the destination node was introduced. In paper [22], a design and implementation based on FPGA for the detector at the destination node in a MIMO-SDM-PNC system was proposed.

This paper aims to design and implement the signal processing unit at the relay node based on FPGA for the MIMO-SDM-PNC system proposed in [14] which uses both zero forcing (ZF) and minimum mean square error (MMSE) detector. In the proposed architecture, structure of the arithmetic and matrix calculation modules is designed to work with complex numbers. In order to improve the system throughput, the pipeline technique and parallel processing are jointly combined to implement associated modules. In our design, there are several associated types such as matrix addition, matrix multiplication, matrix Hermit transformation and matrix inversion. Among these modules, the matrix inversion module requires a large number of calculations and a large amount of calculation time. We propose some designs for this module and analyze them to find out an optimal solution.

The rest of this paper is organized as follows. System model of the considered system is illustrated in Sec. II. The FPGA architecture and some main modules are presented in Sec. III. Sec. IV presents implementation results and finally Sect. V concludes the paper.

II. System Model

In this paper, we consider a MIMO-SDM-PNC two-way relay system similar to that in [14] which is illustrated in Fig. 1. In this system, the two source nodes N_1 and N_2 exchange data via the relay node R. Each source node has two transmit antennas and two receive antennas while the relay node has 2 transmit antennas and 4 receive antennas. We assume that all nodes operate in the half-duplex mode and there is no direct link between the source nodes. The transmission in the two-way system consists of two phases. In the first phase period, two node N_1 and N_2 simultaneously send data streams $\boldsymbol{x}_1$ and $\boldsymbol{x}_2$ to the relay node R. When the relay node receives the two data streams it encodes them in the PNC form. At the seconds phase, the relay node R broadcasts the encoded data streams to both source nodes.

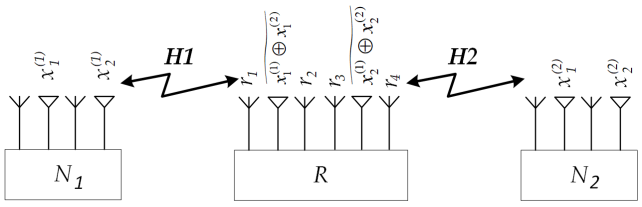

Fig. 1. System model of the MIMO-SDM-PNC two-way relay system.

The two parallel data streams transmitted from the source nodes N_1 and N_2 are given by

$$\boldsymbol{x}_1 = (x_i^{(1)})^{1\times 2}, \qquad \boldsymbol{x}_2 = (x_j^{(2)})^{1\times 2}, \ i,j = 1..2. \quad (1)$$

The channel matrices representing the fading links between the two source nodes and the relay node are denoted by

$$\boldsymbol{H}_1 = (h_{ij}^{(1)})^{4\times 2}, \quad \boldsymbol{H}_2 = (h_{nm}^{(2)})^{4\times 2}, \quad (2)$$

where $i,n = 1,2$; $j,m = 1,2,3,4$.

The equivalent channel matrix and equivalent transmit signal vector can be represented as follows

$$\boldsymbol{H} = [\boldsymbol{H_1},\ \boldsymbol{H_2}]; \quad (3)$$

$$\boldsymbol{x} = [\boldsymbol{x}_1,\ \boldsymbol{x}_2]^T. \quad (4)$$

At the relay node, the received signal vector from the source nodes can be obtained by the following equations.

$$\begin{aligned} \boldsymbol{r} &= \frac{1}{\sqrt{2}}\boldsymbol{H}\boldsymbol{x} + \boldsymbol{n}; \\ &= \frac{1}{\sqrt{2}}\boldsymbol{H}\boldsymbol{V}^{-1}(\boldsymbol{V}\boldsymbol{x}) + \boldsymbol{n}; \\ &= \frac{1}{\sqrt{2}}\hat{\boldsymbol{H}}\hat{\boldsymbol{x}} + \boldsymbol{n}, \end{aligned} \quad (5)$$

where the received signal vector $\boldsymbol{r} = [r_1, r_2, r_3, r_4]^T$ and the noise vector $\boldsymbol{n} = [n_1, n_2, n_3, n_4]^T$; the fraction $\frac{1}{\sqrt{2}}$ is the power normalization factor. The matrix $\hat{\boldsymbol{H}}$ and vector $\hat{\boldsymbol{x}}$ can be defined as

$$\hat{\boldsymbol{H}} \triangleq \boldsymbol{H}\boldsymbol{V}^{-1} \quad (6)$$

$$\hat{\boldsymbol{x}} \triangleq \boldsymbol{V}\boldsymbol{x}. \quad (7)$$

The matrix $\boldsymbol{V}$ is determined as in the paper [14], i.e.

$$\boldsymbol{V} = 2\boldsymbol{V}^{-1} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix}. \quad (8)$$

Therefore, the vector $\hat{\boldsymbol{x}}$ can be rewritten as follows

$$\hat{\boldsymbol{x}} = \begin{bmatrix} x_1^{(1)} + x_1^{(2)} \\ x_2^{(1)} + x_2^{(2)} \\ x_1^{(1)} - x_1^{(2)} \\ x_2^{(1)} - x_2^{(2)} \end{bmatrix}. \quad (9)$$

In order to estimate the vector $\hat{\boldsymbol{x}}$, a low-complexity linear detector is employed. From (9) it is clear that the role of the relay node is to estimate the summation component $x_i^{(1)} + x_i^{(2)}$ and the difference component $x_i^{(1)} - x_i^{(2)}$ (where $i = 1, 2$) from the received signal vector $\boldsymbol{r}$. Using the ZF or MMSE detector [14] the weight matrix is used for linear combining is given respectively by

$$\boldsymbol{G}^{\mathrm{ZF}} = \left(\hat{\boldsymbol{H}}^H \hat{\boldsymbol{H}}\right)^{-1} \hat{\boldsymbol{H}}^H; \quad (10)$$

$$\boldsymbol{G}^{\mathrm{MMSE}} = \left(\hat{\boldsymbol{H}}^H \hat{\boldsymbol{H}} + \sigma_n^2 \boldsymbol{I}_2\right)^{-1} \hat{\boldsymbol{H}}^H; \quad (11)$$

As a result, the vector $\hat{\boldsymbol{x}}$ can be estimated as follows

$$\boldsymbol{y} = \boldsymbol{G}\boldsymbol{r} = \begin{bmatrix} \widetilde{x_1^{(1)} + x_1^{(2)}} \\ \widetilde{x_2^{(1)} + x_2^{(2)}} \\ \widetilde{x_1^{(1)} - x_1^{(2)}} \\ \widetilde{x_2^{(1)} - x_2^{(2)}} \end{bmatrix}, \tag{12}$$

where $\boldsymbol{y} \triangleq \begin{bmatrix} y_1^{(s)} & y_2^{(s)} & y_1^{(d)} & y_2^{(d)} \end{bmatrix}^T$.

The log likelihood ratio (LLR) combination method is used to transform both $x_i^{(1)} + x_i^{(2)}$ and $x_i^{(1)} - x_i^{(2)}$ into the target network coded signal $x_i^{(1)} \oplus x_i^{(2)}$, which is expressed as

$$L(x_i^{(1)} \oplus x_i^{(2)} | y_i^{(s)} y_i^{(d)}) = \frac{P(y_i^{(s)} y_i^{(d)} | x_i^{(1)} \oplus x_i^{(2)} = 1)}{P(y_i^{(s)} y_i^{(d)} | x_i^{(1)} \oplus x_i^{(2)} = -1)}, \tag{13}$$

where $i = 1, 2$.

The LLRs can be calculated from equations (13) as follows [14]:

$$\begin{aligned} \mathrm{LLR}_{S_i} = \exp\left(\frac{-(y_i^{(d)})^2}{2(\sigma_i^{(2)})^2}\right) \times \\ \left[\exp\left(\frac{-(y_i^{(s)}-2)^2}{2(\sigma_i^{(1)})^2}\right) + \exp\left(\frac{-(y_i^{(s)}+2)^2}{2(\sigma_i^{(1)})^2}\right)\right] \end{aligned} \tag{14}$$

$$\begin{aligned} \mathrm{LLR}_{D_i} = \exp\left(\frac{-(y_i^{(s)})^2}{2(\sigma_i^{(1)})^2}\right) \times \\ \left[\exp\left(\frac{-(y_i^{(d)}-2)^2}{2(\sigma_i^{(2)})^2}\right) + \exp\left(\frac{-(y_i^{(d)}+2)^2}{2(\sigma_i^{(2)})^2}\right)\right] \end{aligned} \tag{15}$$

where $\left(\sigma_k^{(i)}\right)^2 = \left(\boldsymbol{G}^H\boldsymbol{G}\right)_{k,k}\sigma_n^2$ denotes the noise variance corresponding to the k-th output stream of the k-th user from the linear detector. The PNC symbol $\widetilde{x_i^{(1)} \oplus x_i^{(2)}}$ is then given by

$$\widetilde{x_i^{(1)} \oplus x_i^{(2)}} = \begin{cases} -1 & \text{if} \quad \mathrm{LLR}_{S_i} \geq \mathrm{LLR}_{D_i} \\ +1 & \text{if} \quad \mathrm{LLR}_{S_i} < \mathrm{LLR}_{D_i} \end{cases} \tag{16}$$

As a result, the PNC symbols can be mapped by using the following rule

$$\widetilde{x_i^{(1)} \oplus x_i^{(2)}} = \begin{cases} \mathrm{sign}(|y_i^{(s)}| - \gamma) & \text{if } (\boldsymbol{G}\boldsymbol{G}^H)_{i,i} < (\boldsymbol{G}\boldsymbol{G}^H)_{k,k} \\ \mathrm{sign}(\gamma - |y_i^{(d)}|) & \text{otherwise} \end{cases} \tag{17}$$

where γ is the decision threshold which can be selected optimally, and $k = i+2$. Fig. 9 and Fig. 10 show the simulation results using linear detection based on ZF an MMSE detector, respectively [14].

III. Hardware Architecture

Based on Eqs. (10), (11), we propose a hardware architecture of the digital processing unit for the MIMO-SDM-PNC two-way relay system based on the ZF and MMSE detector as illustrated in Fig. 2 and Fig. 3, respectively. The architecture is designed to take advantages of the FPGA, namely pipeline computing and parallel operation. Moreover, in order to analyze and optimize the proposed architecture, both conventional and proposed architectures will be evaluated and compared with each other. After that, the parameters of the optimal architecture such as the number of quantization levels, normalization factor of divider are estimated to obtain the optimal values.

In the proposed architecture, the set of inputs to the detector are channel matrices denoted by $\boldsymbol{H}_1$, $\boldsymbol{H}_2$ from two source nodes N_1, N_2 to the relay node R, respectively, the received signal vectors at the relay node R and the noise variance σ_n^2 at the destination node in case of using the MMSE detector. These inputs can be fetched at every rising edge of the system clock pulse.

In order to achieve high-speed signal processing for the inputs, pipeline computing and parallel operation are employed in the proposed architecture. The operation of the proposed architecture is described as follows. Firstly, the fading channel matrices $\boldsymbol{H}_1, \boldsymbol{H}_2$ are passed through two modules "Combination" and "$\boldsymbol{H}\boldsymbol{V}^{-1}$" to obtain $\boldsymbol{H}$ and $\hat{\boldsymbol{H}}$ as given by Eqs. (3) and (6), respectively. $\hat{\boldsymbol{H}}$ is then transformed to $\hat{\boldsymbol{H}}^H$ by the "Hermitian Transposition" module. Delay is introduced when the data passes though the "Combination", "$\boldsymbol{H}\boldsymbol{V}^{-1}$ " and "Hermitian Transposition" modules, each with one period (T). As a result, $\hat{\boldsymbol{H}}$ and $\hat{\boldsymbol{H}}^H$ data arrive the Matrix Multiplier module. Secondly, the output of "Matrix Multiplier" module $\boldsymbol{H}\boldsymbol{H}^H$ is obtained after four system clocks. In the case of designing the ZF detector, the value of$\boldsymbol{H}\boldsymbol{H}^H$ is transferred to the "Matrix Inversion" module. While in the case of the MMSE detector, it is added with $\sigma_n^2\boldsymbol{I}$ which is delayed by five system clocks to guarantee the system's synchronization. The remaining signal processing operations of the two detectors are the same. The output of the "Matrix Inversion" module $\boldsymbol{K}^{-1}$ and $\hat{\boldsymbol{H}}^H$, which are delayed by $(w + c + 20)T_s$ for ZF and $(w+c+21)T_s$ for MMSE. Then, the outputs are passed to "Matrix Multiplier" module to generate the combining weight matrices $\boldsymbol{G}^{\mathrm{ZF}}$ and $\boldsymbol{G}^{\mathrm{MMSE}}$, respectively. Here T_s denotes the system clock period. Finally, the received signal vector from source node is multiplied by the combining weight matrix $\boldsymbol{G}$ to estimate the summation and difference of the received signals from two sources given by (12) and LLR's values in order to produce the decision value of $\widetilde{\boldsymbol{x_1} \oplus \boldsymbol{x_2}}$. As a result, the system latency for ZF and MMSE detector can be respectively calculated as

$$t_d = \frac{w + c + 30}{F} \tag{18}$$

$$t_d = \frac{w + c + 31}{F} \tag{19}$$

Some main modules that basically decide the system performance will be described, evaluated and optimized in following subsections.

A. Multiplier and Divider

In the proposed architecture, the complex divider is used to calculate the inversion of a 4×4 matrix. In this case, the divisor is actually greater than the dividend. The calculation executed

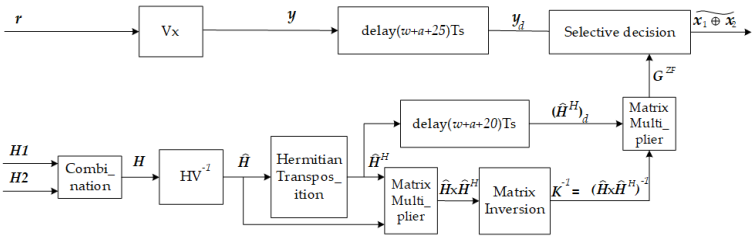

Fig. 2. The architecture of the signal processing unit at the relay node using ZF detector in MIMO-SDM-PNC scheme.

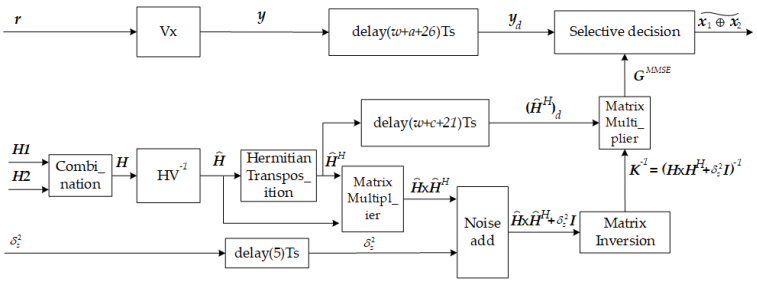

Fig. 3. The architecture of the signal processing unit at the relay node using MMSE detector in MIMO-SDM-PNC scheme.

on the FPGA is integer based. Therefore, the quotient is likely to be zero. For not losing the system channel information, the dividend must be multiplied by a scale factor a as follows

$$2^c a = qb + r, \tag{20}$$

where $a, q, b, r, c \in \mathbb{Z}$. In this paper, the divider is implemented based on pipeline architecture. The divider has $w + c$ stages as depicted in Fig. 4.

The value of the scale factor c is selected corresponding to a defined accuracy. Its maximum value is chosen as the width of the input data bus w.

Operation of the complex number divider is shown in Fig. 5. The result of quotient dividing Q is obtained after $w + c + 4$ system clocks.

B. Complex Matrix Multiplier

In the proposed architecture, the complex matrix multiplier multiplies two complex matrices $\boldsymbol{A}$ and $\boldsymbol{B}$, $\boldsymbol{A} = (a_{ij})^{N\times N}, \boldsymbol{B} = (b_{ij})^{N\times N}$ in which $a_{ij}, b_{ij} \in \mathbb{C}$, $\boldsymbol{C} = \boldsymbol{AB}$, and the elements of $\boldsymbol{C}$ can be calculated as follows

$$c_{nm} = \sum_{k=1}^{N} a_{nk} b_{km}, \ (n, m = 1, 2, ..., N). \tag{21}$$

The 4×4 complex matrix multiplier is constructed by 16 submodules, $N = 4$, as shown in Fig. 6. These submodules are performed in parallel to improve the speed, in other words, to reduce the system latency.

C. Complex Inverse Matrix Calculator

In order to calculate the complex inversion of matrix $\boldsymbol{A} = (a_{nm})^{N\times N}, a_{nm} \in \mathbb{C}$, we assume $\boldsymbol{A}_{nm}$ is a submatrix of matrix $\boldsymbol{A}$ that is made by removing the n-th row and the m-th column of matrix $\boldsymbol{A}$. The minor A_{nm} of the entry in the n-th row and the m-th column and comatrix $\boldsymbol{P}_A$ can be calculated respectively as follows

$$A_{nm} = \det(\boldsymbol{A}_{nm}) \tag{22}$$

$$\boldsymbol{P}_A = ((-1)^{m+n} A_{mn}) = ((-1)^{m+n} A_{nm})^T. \tag{23}$$

If the determinant of matrix $\boldsymbol{A}$ is not equal zero, the inverse matrix of $\boldsymbol{A}$ can be calculated as

$$\boldsymbol{A}^{-1} = \frac{1}{\det(\boldsymbol{A})} \boldsymbol{P}_A. \tag{24}$$

The determinant of matrix $\boldsymbol{A}$ and the minor A_{nn} are calculated as

$$det(\boldsymbol{A}) = \sum_{j=1}^{N-1} A_{1j} det(\boldsymbol{A}_{1j}), \tag{25}$$

$$det(\boldsymbol{A}_{nm}) = \sum_{j=1}^{N-1} (A_{nm})_{1j} det((\boldsymbol{A}_{nm})_{1j}), \tag{26}$$

where $(\boldsymbol{A}_{nm})_{1j}$ is the submatrix of the matrix $\boldsymbol{A}_{nm}$, that is made by removing the 1-th row and the j-th column of the matrix $\boldsymbol{A_{nm}}$. A_{nm} is the element of the matrix $\boldsymbol{A_{nm}}$ at the 1-st row and the j-th column [23], [24]. The proposed architecture to calculate an $N \times N$ matrix's determinant is shown in Fig. 7.

As presented by equations (22)-(26), a proposed architecture of the complex inverse matrix calculator consists of sixteen submodules. Each submodule calculates an element of the inverse matrix in parallel manner. Fig. 8 shows an architecture of submodule that calculates an element A_{nm}^{-1} of matrix $\boldsymbol{A}^{-1}$ at the n-th row and the m-th column without considering the sign value $(-1)^{n+m}$.

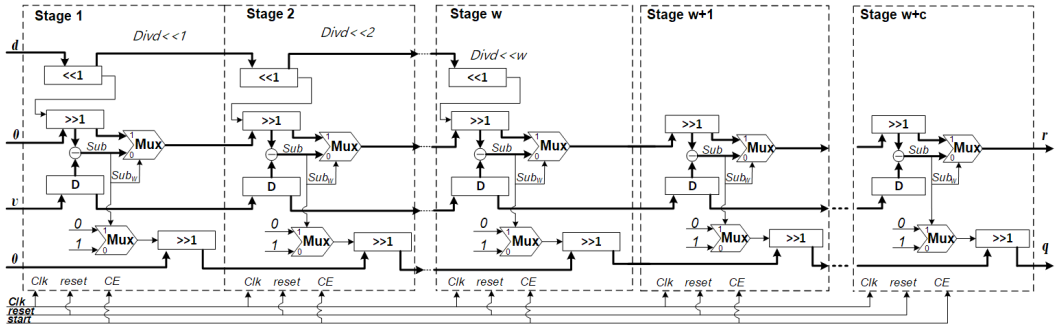

Fig. 4. The architecture of the integer divider.

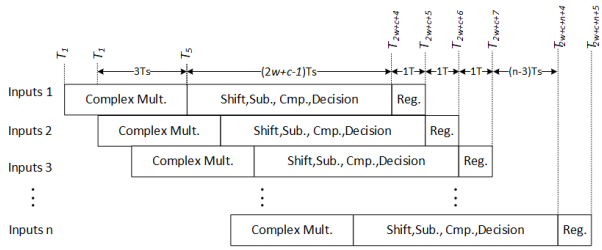

Fig. 5. Pipelining stages of the complex number divider.

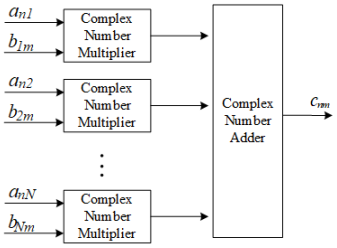

Fig. 6. The architecture of submodule calculating an element of the $N \times N$ product matrix (where $n, m = 1..N$).

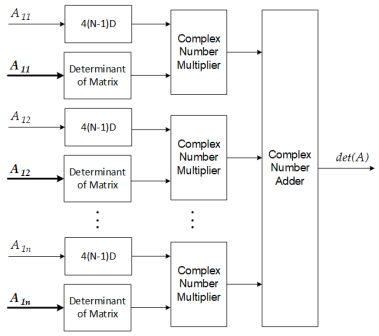

Fig. 7. The architecture of an $N \times N$ determinant calculator

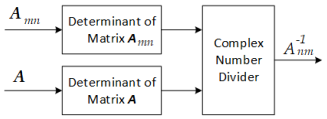

Fig. 8. The architecture of submodule calculating an element of the inverse matrix

IV. Implementation Results

In this section, the MIMO-SDM-PNC scheme is designed and implemented on FPGA with ZF and MMSE detectors. The system parameters are set as followings. The modulation scheme is BPSK. The width of the input data bus is w corresponding to the number of the ADC quantization bits. The scale factor of the divider used in the inverse matrix calculator is c. Firstly, to evaluate numerical performance of the proposed system, a Matlab simulation model which is completely consistent with the hardware implementation is considered. Then the proposed system is synthesized by the Xilinx ISE14.5 tool, in which the chosen IC is the Xilinx Virtex 7 XC7VX1140T FPGA.

Fig. 9 and Fig. 10 demonstrate a comparison of Monte-Carlo simulation results based on the LLR, $Selective$ methods and FPGA implementation $Selective_{\mathrm{FPGA}}$. As can be seen from these figures, bit error rate (BER) of the proposed system implemented on FPGA is close to the simulation results applied LLR, $Selective$ ones in both ZF and MMSE schemes. The system's accuracy depends on the width of the input data bus w and the scale factor c. If w and c are bigger, the $Selective_{\mathrm{FPGA}}$ BER curve becomes closer to the simulation curves, however, the required resource is bigger and the latency is larger.

The pipelining operations and timing diagrams of the proposed MIMO-SDM-PNC detector using ZF and MMSE method are illustrated in Fig. 13, Fig. 14 and Fig. 13, Fig. 14, respectively. The system latency, which is determined from the point of the valid input to the point when the estimated value $\widetilde{x_i^{(1)} \oplus x_i^{(2)}}$ is produced, are $w+c+30$ and $w+c+31$ system clocks for the ZF and the MMSE detectors, respectively.

To evaluate the proposed design, we set the system parameters as shown in Table I and Table II. The parameter w depends on the number of ADC quantization bits and the maximum value of parameter c is chosen by w. The proposed system has been designed and synthesized based on a number of different ADC. As can be seen from Table I and Table II. The hardware usage of the system and the latency increase when the parameters w and c increase. On the other hand, the

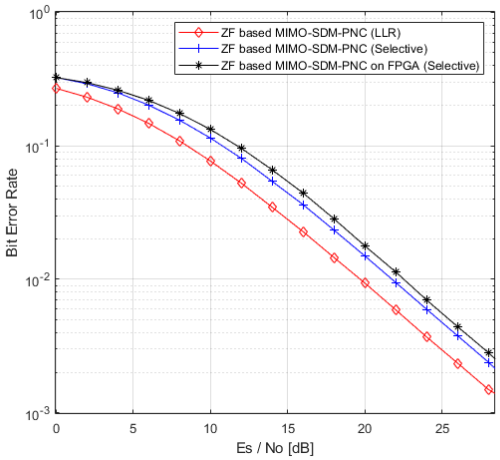

Fig. 9. BER performance of the MIMO-SDM-PNC using ZF.

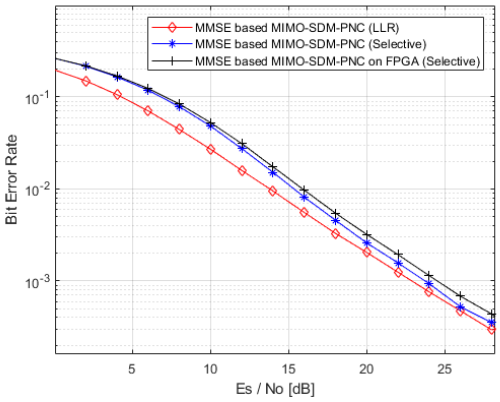

Fig. 10. BER performance of the MIMO-SDM-PNC using MMSE .

maximum frequency and the throughput decrease when the parameters w and c increase as illustrated in Tab. III.

TABLE I
TABLE 1. USED RESOURCE OF MIMO-SDM-PNC USING ZF DETECTOR

w	c	Max Fre. (MHz)	Slice Reg	Slice LUTs	LUT Flip Flop	DSP48E1s
12	6	200.146	19342	22724	28620	1328
12	12	200.146	22084	26238	33179	1328
14	7	199.070	24465	29420	36877	1328
14	14	199.070	28280	34302	43203	1328
16	8	198.006	30088	36388	45616	1328
16	16	198.006	40760	43310	61213	1328
18	9	196.953	41571	44524	62341	1328
18	18	196.953	49896	52846	74952	1328

V. CONCLUSION

In this paper, the MIMO-SDM-PNC system with ZF and MMSE detector was designed and implemented based on the FPGA. Several hardware architectures and designs were analyzed to find out a high-performance solution. Moreover, some main system parameters as the width of data input bus and the

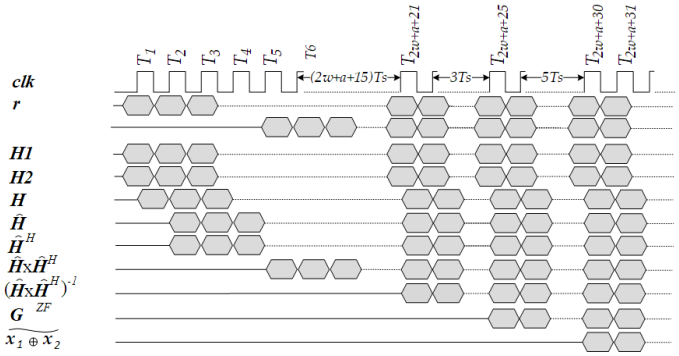

Fig. 11. Timing digram of the detector at the MIMO-SDM-PNC relay node based on ZF detector

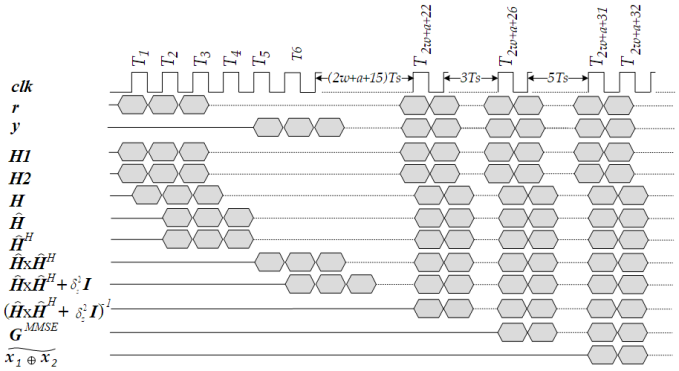

Fig. 12. Timing digram of the detector at the MIMO-SDM-PNC relay node based on MMSE detector

TABLE II
TABLE 2. USED RESOURCE OF MIMO-SDM-PNC USING MMSE DETECTOR

w	c	Max Fre. (MHz)	Slice Reg	Slice LUTs	LUT Flip Flop	DSP48E1s
12	6	200.146	19403	22832	28729	1328
12	12	200.146	22145	26360	33319	1328
14	7	199.070	24536	29546	37004	1328
14	4	199.070	28351	34446	43367	1328
16	8	198.006	30169	36532	45761	1328
16	16	198.006	40841	43472	61376	1328
18	9	196.953	41662	44686	62503	1328
18	18	196.953	49987	53030	75137	1328

TABLE III
TABLE 3. LATENCY AND THROUGHPUT OF MIMO-SDM-PNC USING ZF AND MMSE DETECTORS

w	c	Latency for ZF (ns)	Latency for MMSE (ns)	Throughput for ZF and MMSE (Mbps)
12	6	257.843	244.821	800.584
12	12	286, 492	274.799	800.584
14	7	256.191	261.215	796.280
14	14	291.355	296.378	796.280
16	8	272.719	277.769	792.024
16	16	313.122	318.172	792.024
18	8	289.409	294.487	787.812
18	18	335.105	340.183	787.812

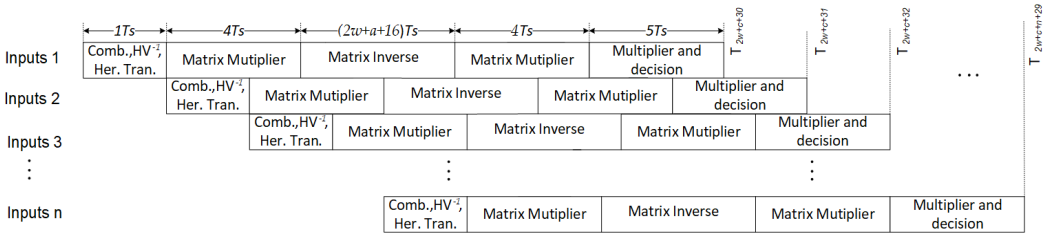

Fig. 13. Pipeline stages of signal processing for MIMO-SDM-PNC based on ZF detector

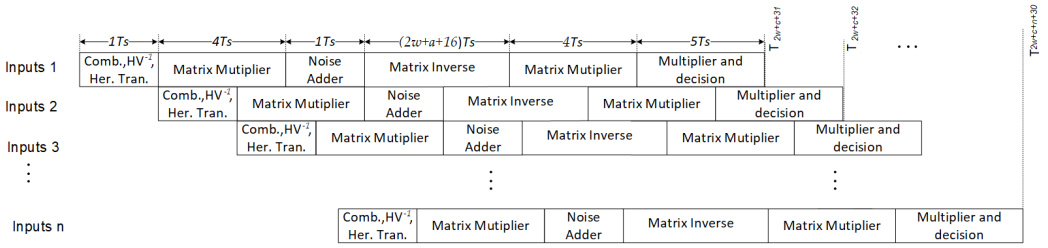

Fig. 14. Pipeline stages of signal processing for MIMO-SDM-PNC based on MMSE detector

scale factor of divider that influenced the system performance were also evaluated. The implementation results demonstrated that the proposed design achieved high throughput and low latency.

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