Design of An Independently Biased Cascode GaN HEMT Microwave Power Amplifier

Luong Duy Manh
Faculty of Radio-Electronic Engineering
Le Quy Don Technical University
236 Hoang Quoc Viet, Hanoi, Vietnam
Email: duymanhcs2@mta.edu.vn

Nguyen Huy Hoang
Faculty of Radio-Electronic Engineering
Le Quy Don Technical University
236 Hoang Quoc Viet, Hanoi, Vietnam
Email: hoangnh@mta.edu.vn

Bach Gia Duong
Electronics and Telecommunication Center
University of Engineering and Technology
Vietnam National University, Hanoi

Ta Chi Hieu
Faculty of Radio-Electronic Engineering
Le Quy Don Technical University
236 Hoang Quoc Viet, Hanoi, Vietnam
Email: hieunda@yahoo.com

***Abstract*—We propose an independently biased technique for improving both efficiency and linearity of a cascode GaN HEMT power amplifier at 2.1 GHz. The designed power amplifier achieves power gain of 16.5 dB, output power of 32 dBm at power added efficiency of 66 % for single-tone operation. For two-tone operation with a spacing of 4 MHz, the designed amplifier can achieve a power added efficiency of 35.8 % and a power gain of 19.7 dB at a third order intermodulation distortion of -35 dBc. These achieved performance makes the designed amplifier to be able to effectively apply to various promising wireless communications applications like Long-Time Evolution (LTE) mobile network or radar and WiFi.**

I. Introduction

Power amplifier (PA) is one of the critical components in the microwave wireless communication systems. In order to effectively operation the system, PAs need to meet various stringent requirements. They must operate for high efficiency, high output power at low distortion level. Basically, PA operates in two major modes: peak and linear. In the peak mode, PA is designed to achieve the highest possible efficiency while in the linear mode, it is designed for low distortion or high linearity. For the peak mode, there are many approaches for improvement of efficiency such as using class D, class E, class F or harmonic termination[1]-[4]. For the linear mode, conventional techniques for improvement of the circuit linearity include feedforward, pre-distortion or Doherty [6]-[8]. It is widely known that, the peak mode PAs have poor linearity while the linear mode PAs exhibit poor efficiency. This means it is hard to achieve both high-efficiency and high-linearity simultaneously. To overcome these drawbacks of PAs, the present study aims to propose a novel solution so that PA can work well in both peak and linear modes while still being compact. It is well known that cascode configuration [5] which is realized by connecting a common source (CS) transistor with a common gate (CG) transistor can offer promising advantages including wide bandwidth, high power gain and high input/output isolation. However, conventional cascode configuration has a drawback of the floating potential point between two transistors. This issue causes an instability for the circuit resulting in degradation of the PA performance. To resolve this problem, an independently biased technique will be employed. This technique is realized by inserting an additional bias terminal to the common point between two transistors [9][10] as shown in Fig. 1. Owing to this technique, operation condition of each transistor can be controlled independently resulting in an ability of both efficiency and linearity improvement. The paper is organized as follows: Sec. II will give the detailed design procedure and discuss the simulated results of the independently biased cascode GaN HEMT power amplifier and Sec. III will conclude the paper.

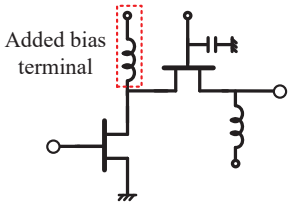

Fig. 1. Independently biased cascode configuration.

II. Design procedure

A. General consideration

In this paper, GaN HEMT model is from Win Semiconductor Inc. with a gate width of 75 μm and 4 fingers. The main purpose of this paper is to design a microwave power amplifier based on this GaN HEMT which has good efficiency and high linearity. Hence, the first transistor of the cascode configuration is biased near class B operation ($V_{DS} = 6V, V_{GS} = -2.9V$) for high efficiency while the second transistor is biased near class AB operation ($V_{DS} = 34V, V_{GS} = -2.5V$) for improvement of the linearity. In order to improve the circuit efficiency, harmonic termination methods will be utilized in this paper.

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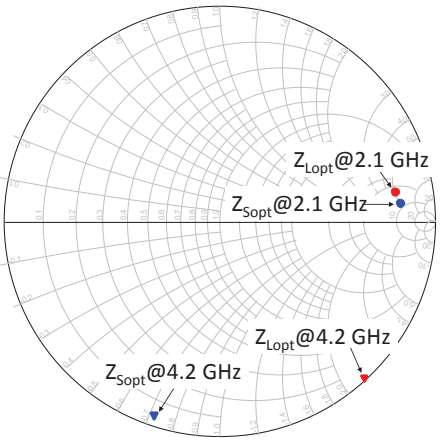

Fig. 2. Simulated optimum load and source impedances realized using load/source pull technique.

This method can be expressed via the following equation for the voltage and current at the transistor:

$$v_{\mathrm{DS}}(t) = V_0 + \sum_{\mathrm{n}=1} \sqrt{2} V_{\mathrm{n}} \sin(\mathrm{n}\omega_0 t + \Phi_{\mathrm{n}}) \tag{1}$$

$$i_{\mathrm{DS}}(t) = I_0 + \sum_{\mathrm{n}=1} \sqrt{2} I_{\mathrm{n}} \sin(\mathrm{n}\omega_0 t + \Phi_{\mathrm{n}} + \phi_{\mathrm{n}}) \tag{2}$$

Therefore, the average power dissipation on transistor can be calculated as:

$$P_{\mathrm{a}} = \frac{1}{T} \int_0^T v_{\mathrm{DS}}(t)\, i_{\mathrm{DS}}(t)\, dt = V_0 I_0 + \sum_{\mathrm{n}=1} V_{\mathrm{n}} I_{\mathrm{n}} \cos\phi_{\mathrm{n}} \tag{3}$$

From this, to minimize power dissipation on transistor or maximize the efficiency, two following conditions must be fulfilled simultaneously:

$$V_0 I_0 + V_1 I_1 \cos\phi_1 = 0 \tag{4}$$

$$\sum_{\mathrm{n}=2} V_{\mathrm{n}} I_{\mathrm{n}} \cos\phi_{\mathrm{n}} = 0 \tag{5}$$

condition (4) means all DC supplied power is transferred to the fundamental output signal while condition (5) indicates that all harmonics must be suppressed. In this paper, we fulfill these conditions by using a load/source pull technique which is embedded in the Keysight ADS 2011.01 simulator. By using such a technique, optimum impedances at fundamental and second harmonic frequencies at both source and load size which satisfy (4) and (5) are shown in Fig. 2. It can be seen in the figure that, the optimum second harmonic impedances locate around the boundary of the Smith chart indicating a purely reactive component. This means phase difference between voltage and current at the transistor is $\pm\pi/2$ satisfying condition (5) for the second harmonics. Condition (4) for the fundamental frequency is satisfied with the above optimum fundamental impedances at 2.1 GHz. After determining the optimum impedances, the next design step is going to design matching networks and biasing network. In the present study, matching and biasing networks are implemented using

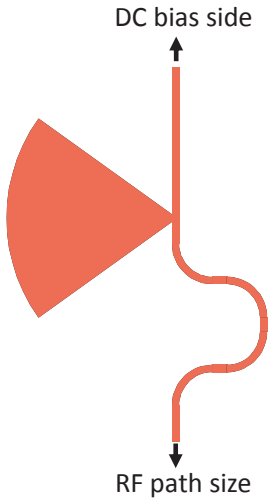

Fig. 3. EM model of the biasing circuit.

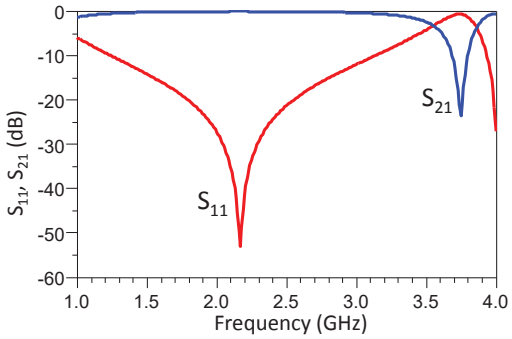

Fig. 4. Simulated S-parameters of the designed bias network.

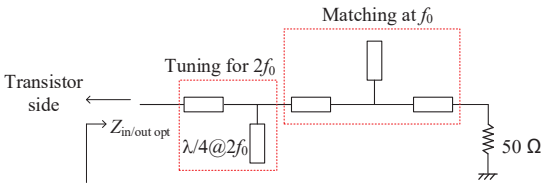

Fig. 5. Matching networks design strategy.

microstrip lines on a Megtron 6 substrate from Panasonic with following parameters: thickness: 0.75 mm; conductor thickness: 0.35 μm; dielectric constant: 3.7; dielectric loss tangent: 0.002. Before designing the input/output matching networks, biasing network will be designed first. The main purpose of the biasing network is to supply DC power to the PA while isolating RF signal from the main signal path.

B. Bias network design

The designed bias network to supply voltages $V_{\mathrm{DS}}, V_{\mathrm{GS}}$ for each transistor is shown in Fig. 3 which the EM model of the circuit. Here, a radial stub functioned as a by-pass capacitor is utilized to widen the bandwidth of the circuit. Moreover, width

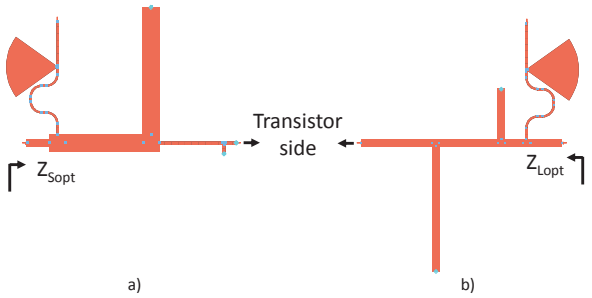

Fig. 6. EM model of the designed matching networks: a) Input matching network and b) output matching network.

of the microstrip line is set narrow to obtain high characteristic impedance. Fig. 4 shows the simulated S-parameters of this designed bias network. It can be seen that the simulated results indicate high S_{21} of -0.04 dB and low S_{11} of -35 dB at 2.1 GHz that validate the accuracy of the bias circuit design.

C. Input/output matching network design

The next step is to design low loss matching circuits to realize the optimum impdedaces at the fundamental and second harmonic frequencies. The strategy to design the matching networks is illustrated in Fig. 5. To realize the terminated purely reactive impedance at the second harmonic or 4.2 GHz, an open stub will be used as a quarter-wave line at 4.2 GHz. In addition, other following transmission lines will be tuned to realize the optimum impedance at fundamental frequency or 2.1 GHz. Fig. 6 shows EM model for the designed input/output matching networks including the designed bias network. The realization of the optimum impedances by these designed networks are indicated in Fig. 7. The figure shows that the EM model can realize the optimum impedances for fundamental and second harmonic quite accurately. Besides the accurate realization of the optimum impedances, the matching networks need to be designed for low loss. In the 50 Ω system, the matching network loss is evaluated by the following equation:

$$\mathrm{IL(dB)} = 10\log\left(\frac{1-|S_{11}|^2}{|S_{21}|^2}\right) \qquad (6)$$

By using the above equation, the insertion loss of the designed matching networks are shown in Fig. 8. The figure shows that at 2.1 GHz, the insertion loss of the input and output matching networks are 0.2 dB and 0.3 dB, respectively. After all components of the PA have been correctly designed, the entire circuit will be evaluated for its performance under the large-signal operation. The entire circuit schematic which will be used for co-simulation is illustrate in Fig. 9. In this circuit schematic, other remaining components in the circuit like DC block and RF by-pass capacitors are used with realistic models from Murata Manufacturing Co. The bonding wires are used using a default library in the ADS simulator.

D. Simulated results

Finally, the co-simulated one-tone and two-tone results are indicated in Fig. 10 and Fig. 11, respectively. Fig. 10 shows

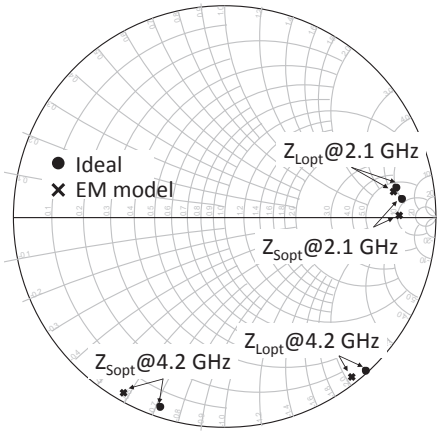

Fig. 7. Realization of the optimum impedances by the designed matching networks.

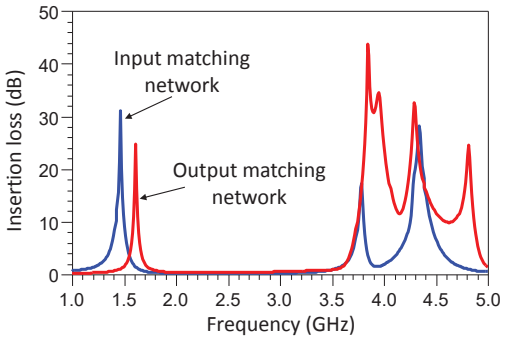

Fig. 8. Simulated insertion loss characteristic of the input/output matching network.

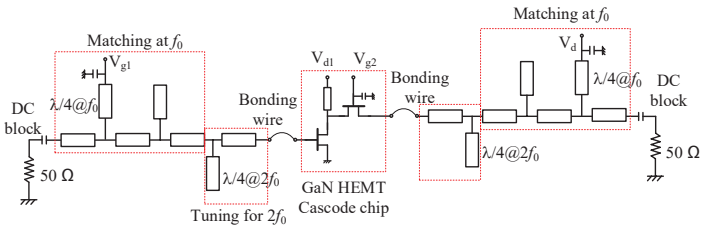

Fig. 9. Entire circuit schematic for co-simulation.

that in one-tone operation, the designed PA can deliver a maximum PAE of 66% and Gain of 16.5 dB at an output power of 32 dBm. Fig. 11 shows that in two-tone operation with a spacing of 4 MHz, the designed PA can achieve PAE of 35.8 % and a power gain of 19.7 dB at IMD3 of -35 dBc. These results confirm the validation of the designed PA with both high efficiency and low distortion. In order to further validate the design, the proposed PA performance is compared with that of a conventional cascode PA. This conventional cascode PA is realized by disconnecting the added bias terminal from the proposed PA. It can be seen in the Fig. 12 which shows the one-tone results comparison that although Pout and Gain of the two PAs are similar, maximum efficiency of the proposed

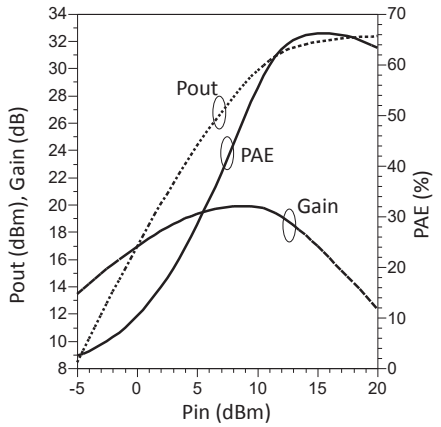

Fig. 10. Simulated one-tone results at 2.1 GHz.

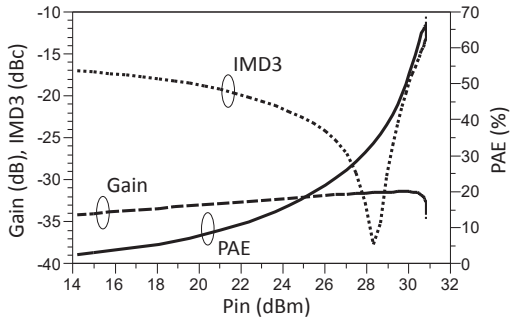

Fig. 11. Simulated two-tone results at 2.1 GHz and a spacing of 4 MHz.

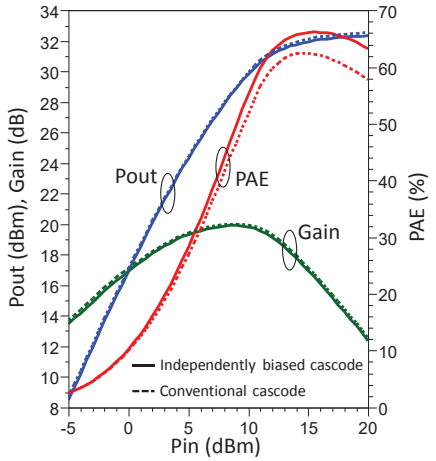

Fig. 12. Comparison of one-tone results between the independently biased cascode and the conventional one.

PA is higher than that of the conventional PA about 4 %. Moreover, from Fig. 13 which shows the two-tone results that the proposed PA exhibit lower IMD3 at higher efficiency region. In addition, at the same IMD3 of -35 dBc, PAE of the proposed PA is higher than that of the conventional PA 5.8 %. This demonstrates that the independently biased

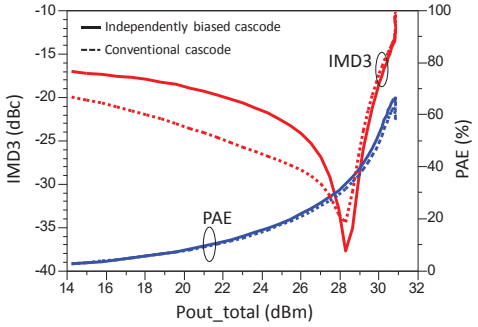

Fig. 13. Comparison of two-tone results between the independently biased cascode and the conventional one.

configuration exhibits superior performance of high efficiency and low distortion over the conventional cascode configuration.

III. Conclusion

In this paper, we have designed a high performance microwave PA at 2.1 GHz based on the independently biased technique. By using the proposed technique, both efficiency and linearity of the PA can be simultaneously improved. When operating under one-tone condition, the proposed PA can deliver a maximum PAE of 66% and Gain of 16.5 dB at an output power of 32 dBm. In the two-tone operation with a spacing of 4 MHz, it can achieve PAE of 35.8 % and a power gain of 19.7 dB at an IMD3 level of -35 dBc. Additionally, performance of the proposed PA has been compared with that of the conventional cascode PA. The compared results indicated that the proposed offers superior efficiency and linearity over the conventional one.

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