Hardware Implementation of Background Calibration Technique for TIADCs with Signals in Any Nyquist Bands

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***Abstract*—In this work, we investigate a novel fully digital background calibration technique to mitigate the gain and timing mismatches in Time-Interleaved Analog-to-Digital Converters (TIADCs) for the wideband bandlimited input signal at any Nyquist zones. The correction scheme is simple by subtracting the image signals from the distorted signal. The channel mismatch parameters are estimated based on out-of-band error estimation. Neither an additional reference channel and nor a pilot input are required in calibration. A four-channel 60dB SNR TIADC operating at 2.7GHz is used in both simulation and experimental implementation to validate the proposed calibration technique. The SNDR improvement is 16dB for a multi-tone input occupied at the third Nyquist band. The calibration method is validated on Altera FPGA DE4 board. In a Hardware-In-the-Loop emulation framework, the synthesized circuit works effectively and utilizes a very little amount of the hardware resource in the FPGA chip.**

I. Introduction

Present-day applications such as cable TVs, optical communications and satellite communications require highly effective analog-to-digital converters (ADCs) having a high resolution and a high sampling rate. In order to achieve these goals, a Time-interleaved ADC (TIADC) which is formed by several time-interleaved ADCs, are imposed [1]. However, the disadvantage of such time-interleaved architecture is that the channel mismatches, even slight, between the individual converters result in parasitic frequency bands possibly occupied in the frequency zone of the wanted signals, limiting the possibilities of employing this technique [2].

Recently, analog and/or mixed signal calibration techniques proposed [2], [3] exhibit good performance. The analog correction schemes however require additional development time and are not portable between CMOS technology nodes. By taking the advantages of CMOS technology scaling, all-digital techniques published in [4]–[8] are the good candidates to overcome the issues of the analog and mixed-signal calibration. There are a few works proposed in [4], [6], [7], coping with the channel mismatches in TIADCs for the input at any *Nyquist Zone (NZ)*, also defined as *Nyquist Band (NB)*. The calibration technique in [6] requires an additional channel and the approach reported in [7] uses a pilot input signal. A background calibration algorithm proposed in [4] minimizes the correlation between the compensated signal and the image signals by effectively forcing the zero-crossings in the compensated signals and image signals due to the channel mismatches, thus minimizing the timing errors. This calibration is heavily relied on the statistics of the input signal [2]. In order to relax the requirements for the input statistical properties, the channel mismatch calibration in [8] proposed the free-band based estimation where the bandlimited input is assumed to be slightly oversampled, generating a frequency band that contains only errors due to the channel mismatches without the input. The frequency band is called free-band or mismatch band. A least mean square (LMS) algorithm is used for minimizing the errors in free-band to estimate the channel mismatch parameters. However, this calibration is limited to the applications with input at the first NZ. Leveraging the technique mentioned in [8], the presented work extends it to the signals located in any Nyquist Band. In addition, we design and validate the proposed mechanism on a field-programmable gate array (FPGA) platform.

The rest of the paper is organized as follows. Section II analyses the limitations of the gain and timing mismatch impact on the TIADC. Section III is dedicated to propose the gain and timing mitigation technique in the TIADC for input located at any NBs. Section IV proposes the optimal hardware architecture in order to validate it on the FPGA platform. Section V shows the experimental results. Finally, the conclusion and future direction are drawn in Section VI.

II. Time-interleaved Analog to Digital Converters

Fig. 1 shows the block diagram of an M-channel TIADC with gain and timing mismatches. g_m and $r_m T_s$ denote the gain and timing mismatches in the m^{th}-channel, where r_m presents the relative timing mismatch and T_s is the overall sampling period. The input signal $x(t)$ is fed into each channel where it is multiplied by g_m and then is sampled at instant time of $(lM+m)Ts+r_m T_s$, generating a sequence $y_m[l]$. The data streams $y_m[l]$ from all channels are combined by a multiplexer (MUX) to generate an output sequence $y[n]$. As the result, the effective sampling period of $y[n]$ is T_s.

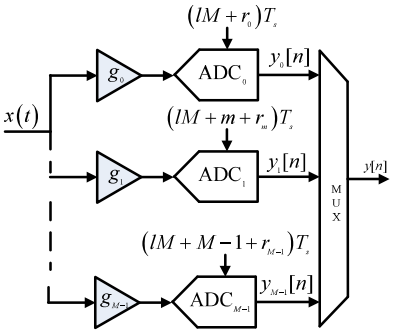

Fig. 1: An M-channel TIADC with gain and timing mismatches.

By assuming a bandlimited input $x(t)$, i.e., $X(j\Omega) = 0$ for $|\Omega T_s| \geq \pi$, the discrete-time Fourier transform (DFT) of the output $y[n]$ can be expressed as [8]

$$Y\left(e^{j\omega}\right) = \sum_{k=0}^{M-1} X\left(e^{j(\omega-\frac{2\pi k}{M})}\right) \breve{H}_k\left(e^{j(\omega-\frac{2\pi k}{M})}\right) \tag{1}$$

where $X\left(e^{j\omega}\right)$ is the discrete-time spectrum of the sampled input $x[n] = x(t)|_{t=nT_s}$ and

$$\begin{aligned} \breve{H}_k(e^{j\omega}) &= \tfrac{1}{M}\sum_{m=0}^{M-1} g_m e^{r_m H_d(e^{j\omega})} e^{-jk\frac{2\pi}{M}m} \\ H_d\left(e^{j\omega}\right) &= j\omega, \text{for} -\pi < \omega < \pi \end{aligned} \tag{2}$$

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$H_d\left(e^{j\omega}\right)$ is the frequency response of an ideal derivative filter [9]. Obviously from (1), if the TIADC has channel mismatches, the

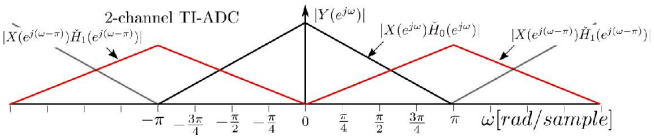

Fig. 2: The Spectrum of the TIADC output for $M = 2$.

output spectrum consists of the original spectrum $X\left(e^{j\omega}\right)$ multiplied by $\breve{H}_0\left(e^{j\omega}\right)$, and frequency-shifted versions of the products $X\left(e^{j\omega}\right)\breve{H}_k\left(e^{j\omega}\right)$ as shown in Fig. 2. The frequency-shifted products are referred to be as the image signals due to channel mismatches that need to be mitigated.

III. Proposed Calibration Technique for Signals in any Nyquist Zone

A. Digital Correction

Without loss of generality, we assume that the average value of the timing mismatches to is zero. In order to be ease of the notation, the average (denoted G_0) of gain mismatch across all channels is assumed to be 1, otherwise the compensated signal is $G_0 x[n]$. In practical TIADCs, the clock skews r_m are typically small compared to T_s. By exploiting the Taylors series approximation and neglecting the high order components, the inverse DFT of (1) can be written as [8]

$$y[n] = x[n] + e[n]. \tag{3}$$

where $e[n]$ is the error due to the gain and timing mismatches. It can be expressed as a sum of two inner-product components:

$$e[n] = c_g^T \mathbf{x}_{g,n} + c_r^T \mathbf{x}_{r,n}, \tag{4}$$

where signal vectors are defined as

$$\begin{aligned} \mathbf{x}_{g,n} &= \mathbf{m}_n x[n] \\ \mathbf{x}_{r,n} &= \mathbf{m}_n \left(h_d[n] * x[n]\right). \end{aligned} \tag{5}$$

$h_d[n]$ is the impulse response of the ideal derivative filter. Symbol T notates the matrix transpose operator. c_g, c_r are column vectors whose elements are the gain and clock skew coefficients, respectively. They are defined in Eq. 12 of [8]. The modulation vector $\mathbf{m}_n$ is expressed in Eq. 13 of [8].

From (4) and (5), the input derivative is required to recover the error signal due to the gain error and timing skew. This derivative is computed by a fixed ideal differentiator filter $h_d[n]$. Regarding bandpass (BP) RF input at higher NZs, a TIADC processes an analog input signal located above the first NB. The frequency range of the first NZ is defined $\left[0, \frac{f_s}{2}\right]$. The analog BP input signal is passed through an TIADC to generate the output data stream. The BP sampling process folds the input signal back to the first NZ (or baseband) as illustrated in the Fig.3. Obviously, the odd-order bandpass sampling makes the shape of both the base-band and the original spectrum identical as shown in Fig. 3(b). For even-order undersampling process, the base-band frequency spectra is inverse to the original input spectrum as described in Fig. 3(a). Thus, the derivative filter $h_d[n]$ need to be re-designed in the channel mismatch calibration for input at higher NBs. Considering a bandpass input signal located at K-th Nyquist band, its 1st-order derivative is expressed as [4].

$$x'[n] = y'[n] + (-1)^K \left\lfloor \frac{K}{2} \right\rfloor 2\pi \hat{y}[n] \tag{6}$$

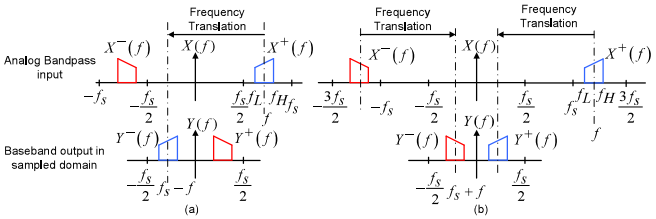

Fig. 3: An example of undersampling the bandpass signal in (a) even order NZ and (b) odd order NZ.

where $\hat{y}[n]$ is the Hilbert transform of $y[n]$. From (6), a filter consisting of the base-band derivative filter $h_d[n]$, a FIR Hilbert filter and a scaling factor of $(-1)^K \left\lfloor \frac{K}{2} \right\rfloor 2\pi$ is used to calculate the derivative of inputs at any NZs. Physically, an additional Hilbert transformer is an all-pass filter that shifts the input signal phase by 90^0 [9]. It covers the bandwidth of the signal to be phase shifted as illustrated in the even-order BP sampling.

In blind calibration, the input is unknown and the output is thus used instead of input for approximation. From (4), (5) and (6), the proposed digital correction technique for signals at any NZs is shown in the left-side of Fig. 4. $h_h[n]$ is a impulse response of the Hilbert filter. It is defined in [9].

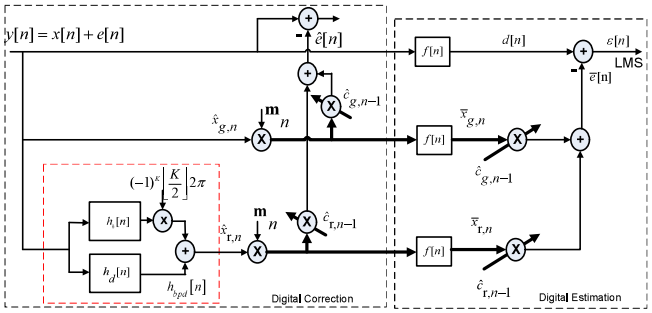

Fig. 4: All-digital gain and timing mismatch mitigation technique for input at any NB.

B. Digital Estimation

In order to estimate the vectors $\{c_g, c_r\}$, Vogel *et al.* in [8] assumes that the input signal is a bandlimited low-pass signal inside the first NZ and that the TIADC slight oversamples the input. Oversampling produces a higher frequency band so-called mismatch band that is free of signal content. This frequency band will only contain the energy of image signals that arise from the error spectra due to the gain and timing mismatches as shown in Fig. 5. Thus, the out-of-

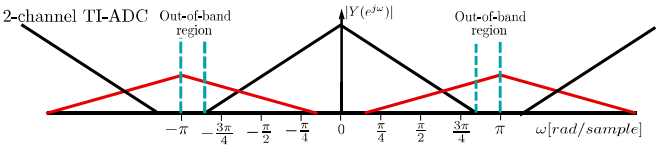

Fig. 5: The Spectrum of the TIADC output for $M = 2$ with the present of out-of-ban region (so-called mismatch band).

band region (so-called mismatch band) contains only error spectra. Note that as the bandlimited signal is in higher NB, the TIADCs use the undersampling technique to sample the input. Thus, the

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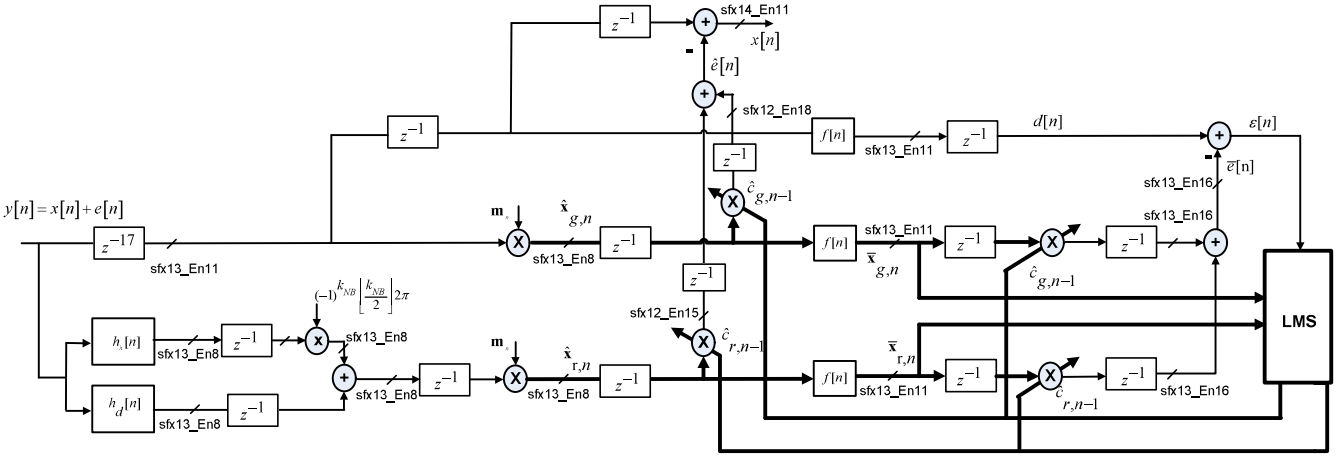

Fig. 6: Hardware Implementation Architecture

above presented mismatch band is copied back the first NZ [9], [10]. Minimizing the error signals in this mismatch band by LMS algorithm is to estimate the gain and timing mismatch coefficients $\{c_g, c_r\}$. The filters $f\,[n]$ diminish the input signal energy and pass only the image energy in the mismatch band. The estimated vectors $\hat{\mathbf{x}}_{g,n}$ and $\hat{\mathbf{x}}_{r,n}$ are also filtered through $f\,[n]$ to generate $\{\bar{\mathbf{x}}_{g,n}, \bar{\mathbf{x}}_{r,n}\}$. The LMS algorithm presented in [8] is used to minimize the error signal $\varepsilon[n] = d[n] - \bar{e}[n]$, and then the updating equations are shown as [8]

$$\begin{aligned} \hat{c}_{g,n} &= \hat{c}_{g,n-1} + \mu_g \bar{\mathbf{x}}_{g,n}^T \varepsilon\,[n] \\ \hat{c}_{r,n} &= \hat{c}_{r,n-1} + \mu_r \bar{\mathbf{x}}_{r,n}^T \varepsilon\,[n], \end{aligned} \tag{7}$$

where μ_g and μ_r are the step size parameters. It would be worth noting that the channel mismatch coefficients are updated by an amount being cross-product of two error signals (the channel mismatch induced image signals and their estimates), hence relaxing the requirements of the input statistical properties [2], [11].

IV. The Proposed Optimal Hardware Architecture

FPGA implementation using Matlab/Simulink in [4] is applied in this framework. The hardware architecture of the proposed calibration is designed and optimized in terms of fixed-point representation of signals that is characterized by signal ranges and signal *Word-Length* (WL). So the parameters of the Optimal Fixed-point Simulink (OFpS) model that need to be optimized, are the order of FIR filters and the signal WLs. The signal ranges of block signals in the OFpS model are mathematically computed based on the transfer function of DSP blocks and simulations as done in [4]. The signal ranges and signal WLs would determine the fractional bits (or precision) used to convert signal values into a binary representation. The OFpS model (or hardware architecture) processes real-time signal data in sample-by-sample manner. Therefore, the delays of each signal datapath are made balanced. Note that, pipeline registers are inserted to reduce the combinational path length and improve the global working frequency and throughput [10]. Fig. 6 shows the pipelined OFpS architecture of the proposed calibration. z^{-k} blocks are delayed/pipeline registers. The notation of $\mathrm{sfix13\_En11}$ presents a 13-bit signed fixed-point data type with a Fraction Length (FL) or fractional bits of 11, i.e., $\mathrm{WL} = 13$ bits and $\mathrm{FL} = 11$ bits. Generally, the representable fixed-point number is actually bounded by $(-2^{\mathrm{WL}-1-\mathrm{FL}},\ (2^{\mathrm{WL}-1}-1)2^{-\mathrm{FL}})$. The TIADC outputs are represented on 13 bits to decrease the sensitivity to digital truncation errors. System-level simulations reveal that the corrected compensated outputs are presented by 14 bits for minimum digital truncation errors. Both the ideal differentiator and Hilbert filter are designed with the optimal FIR order of 30. The LMS block is to update the timing and gain mismatch coefficient estimates expressed in (7). As shown in Fig. 6, the latency between the distorted output and the compensated output is 19 clock cycles.

V. Experimental Results

A. Simulation Results

In simulation, we use an four-channel TIADCs with 60dB SNR (thermal noise level) clocked at $f_s = 2.7$GHz to analyze the efficiency of the proposed calibration technique, The orders of the ideal differentiator and Hilbert filter are chosen to be 30. The coefficients of FIR filters are obtained by multiplying the exact coefficients with a Hanning window. The filters $f[n]$ have 31-taps and the cut-off frequency of 0.8π. They are designed by using *fdesign* function of Matlab. Let us assume the channel mismatches are Gaussian with zero mean and standard deviation of 0.33ps for timing errors and 0.2% for gain error.

Multi-tone BP sinusoid input with $f_L = 3.24$ GHz and $f_H = 3.78$ GHz is generated by simulation as illustrated in Fig. 7. This BP input signal is occupied in the third NB. Sub-sampling TIADC

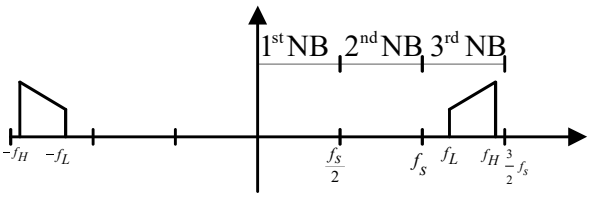

Fig. 7: Nyquist Band (or Nyquist zone) definition

directly down-converts the bandpass input to the frequency baseband $(0, \frac{f_s}{2}) = (0, 1.3\mathrm{GHz})$, i.e., f_L and f_H map to 540MHz and 1.08GHz, respectively as illustrated in Fig. 8. The overall performance of the proposed calibration has been evaluated based on the signal-to-noise-distortion ratio (SNDR) for the uncorrected output given by [8]

$$\mathrm{SNDR} = 10\log_{10}\left(\frac{\sum_{n=0}^{N-1}|x[n]|^2}{\sum_{n=0}^{N-1}|x[n]-y[n]|^2}\right), \tag{8}$$

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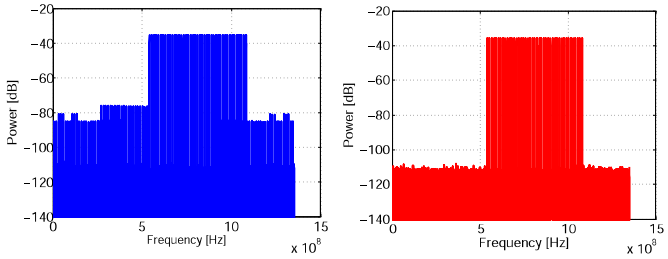
and for the calibrated output given by [8]

$$\mathrm{SNDR} = 10\log_{10}\left(\frac{\sum_{n=0}^{N-1}|x[n]|^2}{\sum_{n=0}^{N-1}|x[n]-\hat{y}[n]|^2}\right), \qquad (9)$$

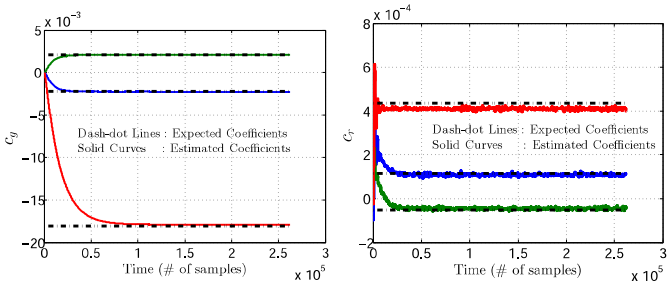
where $y[n], \hat{y}[n]$ are the distorted output and compensated output of TIADC before and after calibration. $x[n]$ is the input of TIADC. The uncalibrated and calibrated output spectra are presented in Fig. 8(a) and (b), respectively. One can observe that the proposed calibration technique cancels out the spurious images due to gain and timing skews in both out-of-band and in-band output spectrum. It improves around 16dB of SNDR. The learning curves of the gain and timing



(a) (b)

Fig. 8: Output spectra for BP input signal with $f_L = 3.24$ GHz, $f_H = 3.24$ GHz in the third NB and $f_s = 2.7$ GHz: (a) before calibration: $\mathrm{SNDR} = 42.37$ dB and (b) after calibration : $\mathrm{SNDR} = 58.45$ dB. (cutoff frequencies of f_L, f_H map to 540 MHz and 1.08 GHz in baseband, respectively.)

coefficients are illustrated in Fig. 9(a) and (b), respectively. The parameter estimates (solid curves) converges to their expected values (dash-dot lines) after around 50K-samples (or 18.5μs).



(a) (b)

Fig. 9: Convergence behavior: (a) gain parameters and (b) timing parameters.

B. Hardware Implementation Results

In order to validate the proposed calibration technique in a hardware platform, Matlab HDL Coder toolbox is used to convert the OFpS model into Hardware Description Language (HDL). Verilog code is generated automatically for the FPGA implementation as well as future ASIC implementation in this framework. The Hardware-In-Loop (HIL) emulation methodology in [4] is applied to validate the proposed calibration on an Altera FPGA board.

The HDL design is systhesized and configured into Altera FPGA DE4 board which contains the Altera Stratix IV FPGA chip EP4SGX230KF40C2. The design is co-simulated in both the FPGA board and the Simulink model in PC. The Simulink HIL model generates the testbench environment by providing the necessary inputs and capturing the outputs of the design in FPGA. The synthesis results show that the proposed calibration circuit operates properly at the maximum clock frequency of 205.4 MHz and consumes very little FPGA hardware resources of 5% logic utilization and 2% DSP 18-bit blocks.

VI. Conclusion

The all-digital background calibration technique is proposed to compensate the gain and timing mismatches in the TIADCs for signal at any NZs. It uses the free-band image estimation scheme to determine the channel mismatches, hence relaxing the requirement of the statistics of the input signal. Moreover, it does not require an additional reference channel and a pilot input. Given the multi-tone input occupied at the third Nyquist zone, the efficiency of the proposed calibration in terms of SNDR is around 16dB for the 4-channel 60dB SNR TIADC clocked at 2.7GHz. The proposed method has worked properly on Altera FPGA DE4 board. The synthesized circuit uses a small amount of hardware resources of the FPGA chip and has the maximum clock frequency of 205.4MHz. In the future, we will provide more comparisons with the state-of-the-art techniques as well as detail ASIC-based implementation results.

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