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Verilog-A Based Compact Model of the Silicon Hall Element

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Abstract— **The paper describes the results of studies devoted to the development and testing of an electric (compact) Hall sensor model. The model implemented in Verilog-A hardware description language provides the capabilities of Hall sensor simulation in Cadence's software environment, taking into account temperature and other effects. Conducted testing of the model showed a satisfactory agreement between the data circuit simulation results of device-technological simulation.**

Keywords— Hall sensor, equivalent circuit, compact model.

I. INTRODUCTION

In the modern electronic equipment magnetic field sensors have a wide application, which are used for magnetic field injection measurements. They are used for car industry, mobile and the other consumer segments – as camera and display sensors, electronic compasses. A significant share in the application of magnetosensitive sensors is occupied by medicine, aerospace and marine industry, energy and the other [1].

One of the most common types of magnetosensitive elements appear Hall sensors (HS). The principle of their action is based on the Hall effect, that is, the emergence of a transverse potential difference when the current flows through a conductor being in a transverse magnetic field. In modern electronics and various technical applications, Hall sensors are used to monitor of movement, position, speed, direction, current, level and other parameters. For these applications, the sensing element (sensor) is integrated into the IC design, i.e., is combined on a single chip with a signal processing circuit [2].

An important problem of the design of integrated sensor systems is that, as a rule, sensitive elements are not included in the design libraries provided by chip manufacturers. I.e. not only the description of the sensor design is missing, but also electric (compact) models intended for circuit simulation of integrated circuits based on it.

A feature of compact models of sensor devices is necessity of a mathematical description of the physical processes occurring in the device structure, taking into account the effect of an external magnetic field.

Currently available models, intended to describe the electrical characteristics of the HS, are either too complex [3] or too idealized [4]. In [3] models based on the use of FEM-like simulators that provide the opportunity of accurate simulation of the electrical characteristics of the sensor, taking into account geometric or structural parameters, as well as the type of active material, are proposed. However, despite the high adequacy of the results, this approach places high demands on computational resources, that limits the possibility of their application for circuit simulation of highly integrated microcircuits.

To achieve reasonable accuracy of circuit simulation of integrated systems based on the HS, it is required to develop an accurate and efficient compact model, based on approaches used for device circuit design consisted standard electronic components. The designed compact model should describe the electrical and operational characteristics of the sensor using the optimal set of equations determined by adequate assumptions and simplifications.

As a means of developing a compact HS model, traditional instruments such as language for circuit simulation SPICE [5], or the hardware description language for analog circuit design Verilog-A [6], should be used. The application of pointed development tools will ensure the simplicity and efficiency of integration of the created models in the design libraries compatible with modern software systems of end-to-end design of integrated circuits.

The paper describes the results of the development and testing of an compact HS model. The model implemented in Verilog-A hardware description language provides the capabilities of HS simulation in Cadence's software [7], taking into account temperature and other effects.

II. HALL SENSOR CONSTRUCTION AND EQUIVALENT CIRCUIT

The symmetrical cross-shaped HS construction (see Fig. 1) is most widely used due to high sensitivity, full compatibility with the standard CMOS process and, consequently, relatively low manufacturing errors. As shown in Fig. 1, the active region of the cross-shaped Hall plate is realized on the low-density n-type region with a concentration of $3{\cdot}10^{16}$ cm^{-3}. Isolation of an n-well with a concentration of $1{\cdot}10^{15}$ cm^{-3} from a p-type substrate is accomplished by a reverse bias of the p-n junction of the well/substrate. To reduce the contact resistance of the contact area, phosphorus is heavily doped to a concentration of $1 \cdot 10^{20}$ cm^{-3} at the stage of creating the source and drain of n-MOS transistors.

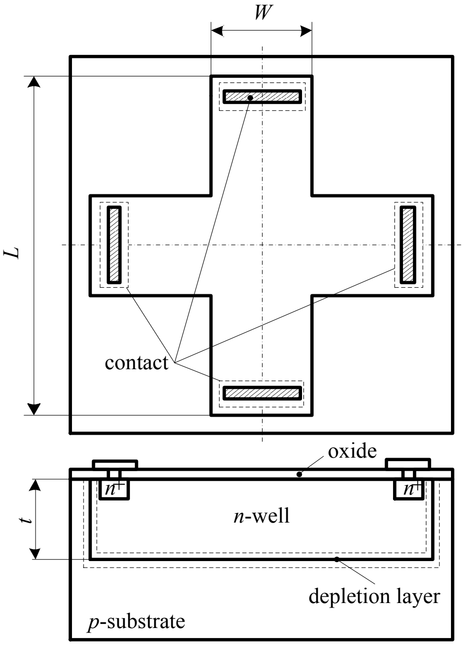

Fig. 1. Symmetrical cross-shaped Hall sensor design.

Below are the equations used to describe the main effects that arise in the structure of the HS: Hall voltage V_H, current-related sensitivity S_I.

The Hall voltage is defined as follows [8] for voltage polarization:

$$V_H = G \cdot r_H \cdot I \cdot B / (n \cdot q \cdot t) \quad (1)$$

where G is the geometrical correction factor, μ_H is the Hall mobility, W and L stand for the width and length of the device respectively, I is the current bias, r_H is the Hall scattering factor, n is the carrier concentration, t is the thickness of the n-well implantation, and B is the magnetic field on a direction perpendicular to the semiconductor probe.

The current-related sensitivity S_I of a HS has the following analytical expression:

$$S_I = G \cdot r_H / (n \cdot q \cdot t) \quad (2)$$

The basic equivalent circuit of the HS [9], shown in Fig. 2, consisting of 4 resistors does not provide sufficiently accurate simulation because of the impossibility of taking into account effects such as thermal and galvanomagnetic effects.

For an ideal design (no technological mismatch, mechanical stress on the device and conduction channel thickness continuously along the device), it is used by the van der Pauw method to measure the surface resistance of the R_S layer. In this condition, since the device is symmetrical, it is necessary to determine two different resistances between the contacts: R_D for the resistance between two opposite contacts and R_H for the resistance between two adjacent contacts [10].

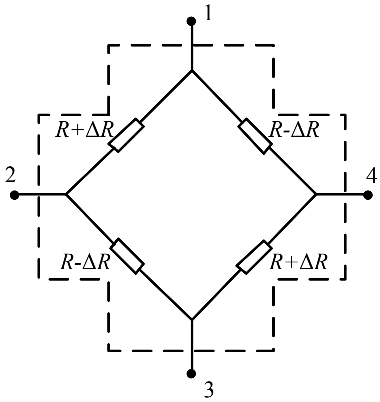

Fig. 2. Basic equivalent circuit for a Hall sensor.

A unified equivalent circuit developed for HS shown in Fig. 3. Using the basic equivalent circuit variant for a cross-shaped HS design consisting of 8 resistors, supplemented voltage sources with a controlled current is proposed. In comparison with the base, this circuit provides higher simulation accuracy by taking into account the galvanomagnetic and temperature effects on the resistance of the n-wells. Four current-controlled voltage sources corresponding to the sensor contacts are designed to describe the Hall voltage.

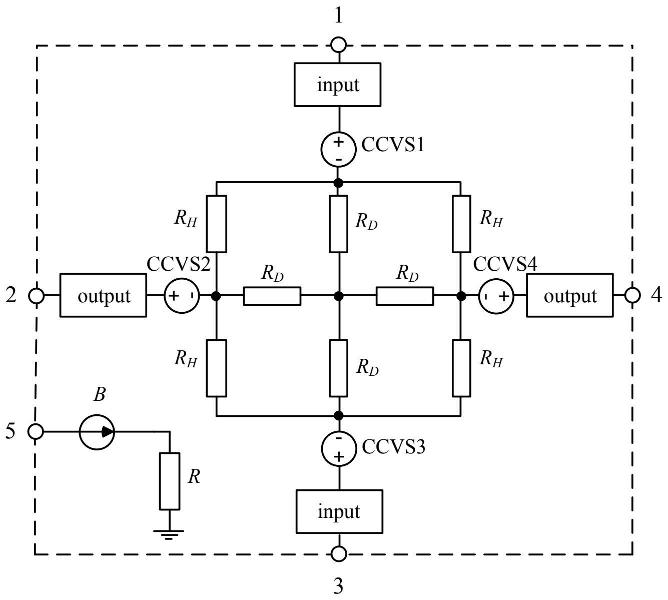

Fig. 3. The model implemented in Verilog-A.

The non-linear resistor is calculated with formula:

$$R = [\alpha + \beta \cdot \exp(\gamma \cdot V)] \cdot [1 + \lambda \cdot (T - T_0)] \cdot (1 + \xi_1 \cdot B + \xi_2 \cdot B^2) \quad (3)$$

where V is the resistor’s internal voltage drop and T_0 is the referent temperature (room temperature). Parameters α, β, γ are extracted from the results of 3D simulations of Hall plates performed for different supply voltages with $B = 0$. The parameter λ is to provide a circuit model able to predict the temperature effects on the HS and their influence on the performance. The last multiplayer term ξ_1 and ξ_2 represents the magneto-resistance effect which becomes important at high magnetic fields.

The resistance of the active sensor region has nonlinear effects that depend not only on the voltage, geometry of the active region, temperature, mechanical stress, but also the magnetic field. In Figs. 4 and 5, the measured input resistance, calculated as a function of the magnetic field induction and temperature. The curves represent linear functions and second-order polynomial.

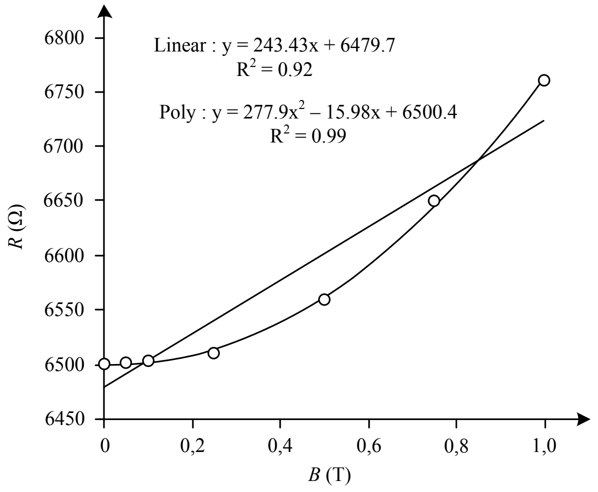

Fig. 4. The input resistance versus the magnetic field.

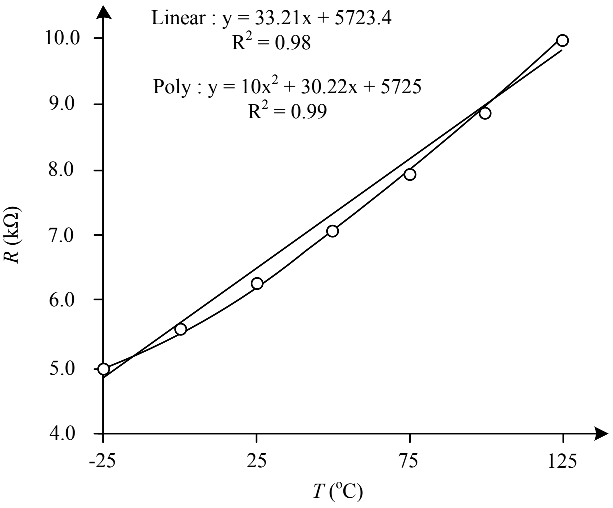

Fig. 5. The input resistance versus the temperature.

III. MODEL REALIZATION

A model of the sensor implemented in the Verilog-A language and includes 4 electrical leads and one external value as an input (B). Inside the model is built by creating instances of three kinds of submodels (see Fig. 3).

Eight nonlinear resistors connected between each pair of contacts and modeled according to the magnetic field and temperature according to (3).

Four current voltage sources (CCVS – Current controlled voltage source) connected to each input contact. The role of these sources is to collect as contributions to the Hall voltage of all the currents flowing through all the nonlinear resistances and to sum them according to (1).

Four interface blocks (input, output) connected to each pin to simulate series resistances.

IV. SIMULATION RESULTS

The Hall voltage, absolute, and current-related sensitivity are some of the figures of merit predicted by simulation for the HS. The temperature influence on the figures of merit governing the sensors performance was also investigated.

Two HS were simulated for various CMOS process technologies. The values of the parameters which used to study HS are presented in Table 1.

TABLE I. SIMULATED HALL SENSORS SIMULATED TECHNOLOGIES

Parameter	**unit**	**Process 1**	**Process 2**
Length L	µm	60	60
Width W	µm	20	20
Thickness t	µm	1.0	1.0
Donor concentration N_D	m^{-3}	$8.0 \cdot 10^{22}$	$3.0 \cdot 10^{22}$
Acceptor concentration N_A	m^{-3}	10^{21}	10^{21}
Conductivity σ	Sm^{-1}	933	383
Mobility µ	$m^2V^{-1}s^{-1}$	0.0715	0.1
R_0 при T=300 К, B = 0 Тл	kΩ	3.1	6.5
S_I	$VA^{-1}T^{-1}$	133	280
Offset drift	µT/°C	0.2	0.13

The model of magnetic elements, developed in Cadence, was used to simulate various integrated HS. All additional blocks that require modeling were coded in Verilog-A.

In order to polarize the Hall cell, we use current bias on the electric path, from left to right. Tensions will be created on the two independent magnetic paths, in the form of a V_{H+} and V_{H-}, respectively. The Hall voltage is therefore the difference of these two potentials

$$V_H = V_{H+} - V_{H-} \qquad (3)$$

This polarization scheme, reconstructed by Cadence's software, is used for the simulation of the sensor (see Fig. 6).

Fig. 7 displays the simulated Hall voltage versus the magnetic field strength, for two integrated Hall elements. For $B = 0.5$ T, the simulated Hall voltage is approximately 71.4 mV (process 2) and 35.9 mV (process 1).

Fig. 8 presents the current-related sensitivity versus the biasing current for both processes. For the same shape and current polarization, a maximization of the current-related sensitivity should be performed by the choice of the carrier concentration. From (2), we can observe that the current-related sensitivity is inversely proportional to n carrier concentration.

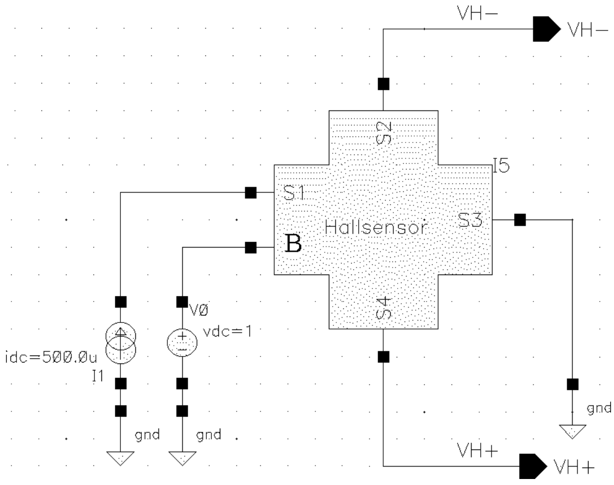

Fig. 6. The model implemented in Verilog-A.

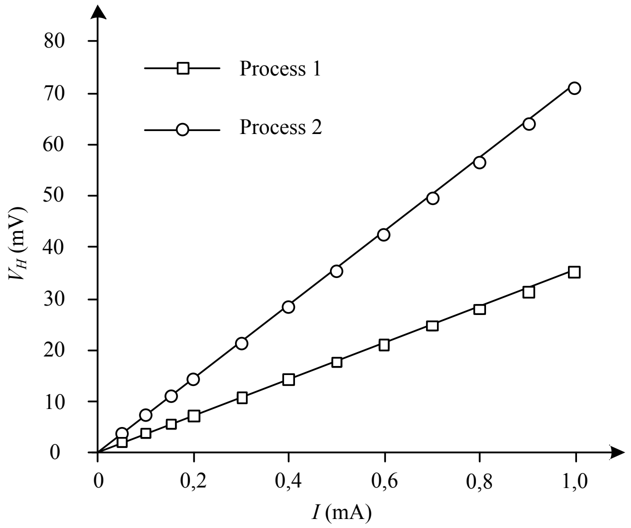

Fig. 7. The simulated output Hall voltage V_H versus the biasing current for two integration CMOS processes at 0.5 T magnetic filed.

The simulated relative variations of the current-related sensitivity related to the value at room temperature as a function of temperature for the zero-stress mounting of the Hall plate is demonstrated in Fig. 9. In this temperature dependence of sensitivity simulation, we assume the zero temperature coefficients λ of Hall plate takes place at 27 °C, and λ linearly changes from -500 ppm/°K to +500 ppm/°K in the temperature range from -25 °C to 125 °C.

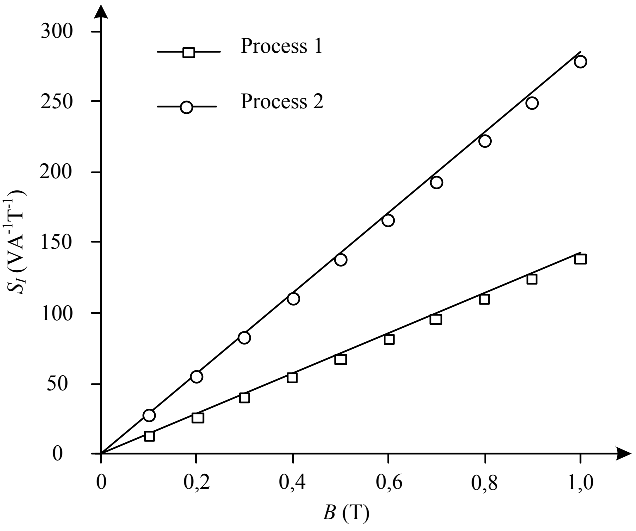

Fig. 8. The simulated current-related sensitivity S_I versus the magnetic field for two integration CMOS processes at 0.5 mA biasing current.

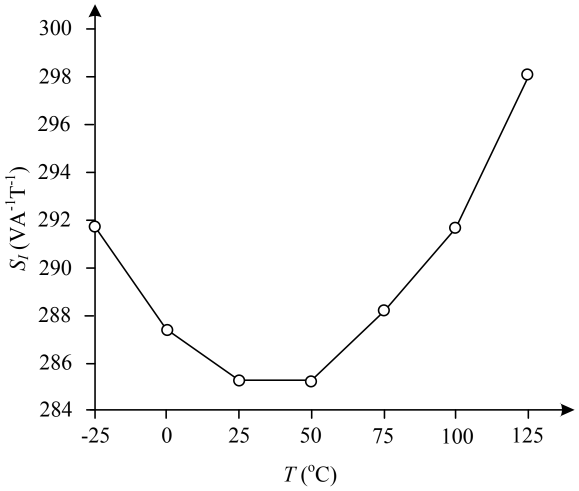

Fig. 9. The simulated current-related sensitivity S_I versus the temperature (process 2).

V. CONCLUSIONS

The compact model of CMOS integrated HS described in this paper has a simple structure which leads to fast simulations while allowing an accurate description of the behavior of the device. It is made of simple sub-components (non-linear resistances, current-controlled voltage sources...) and does not involve any complex equation.

The model involves only sixteen parameters. Eight of them are physical parameters (doping, mobility, depth of n-well, dimensions) and only four are used to fit the contact serial resistances and the process. A straightforward procedure has been established in order to extract these parameters for a given technology. The model, written in Verilog-A, can be easily integrated in a standard CAD tool such as Cadence.

It should be noted that the correction of the model parameters, primarily the mobility, will provide the possibility of its use for simulation of HS вased on other materials, for example wide-gap semiconductors (GaAs, GaN, InP).

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