A New Approach of Stochastic Computing for Arithmetic Functions in Wideband RF Transceivers

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***Abstract*—This paper presents a new approach to approximate various complex arithmetic functions for applications in wideband RF transceivers by using stochastic computing based on the piecewise linear (PWL) approximation. The optimized design parameters for PWL approximation are chosen by an optimization algorithm targeting the best tradeoff between hardware complexity and approximation accuracy. Then, this approximation is implemented by stochastic logic circuits. The proposed approach outperforms previous works based on Maclaurin expansions, Bernstein polynomial and finite-state-machine implementations while achieve similar computation accuracy.**

I. Introduction

Recently, stochastic computing (SC) has attracted many researchers due to its low cost implementation of arithmetic units [1]-[2]. Many applications have employed SC such as artificial neural networks [3], image processing [4], decoding [5] and arithmetic functions computing [6]. In [6], some complex arithmetic functions were efficiently implemented by using Horner's rule for Maclaurin expansions. However, more arithmetic functions with further optimization and more improvements are expected. Moreover, piecewise linear (PWL) approximation has been used as an efficient method to approximate the complex arithmetic functions [7].

On the other hand, in recent years, there has been the remarkable success and growth of high-speed wideband transceivers for wireless communication systems. By taking the benefits of CMOS technology scaling and digital circuits, digitally assistant algorithm can be applied for RF wideband transceiver design. In the receiver chain, the Analog-to-Digital Converter (ADC) is positioned within the front-end chain closer to antenna, as shifting of the analog blocks (filter, mixer and amplifier) to the digital domain to increase the configurability and flexibility of the receivers and known as digital direct-sampling receivers or RF direct receivers. These receivers have only one analog front-end and most of the signal processing functions are performed in digital domain and hence this approach provides scalable and programmable digital tuners. These RF direct receivers require a high speed and low-power ADCs in order to process the wideband signal. The time-interleaved ADC (TIADC) is a promising solution [8]. However, the channel mismatches caused by time-interleaving as well as RF components induced nonlinearity degrade significantly the performance of the receive chain. Thus, all-digital calibration of channel mismatches and linearization technique are required in order to boost further the performance of the receivers. All digital background calibration of channel mismatch in TIADC proposed in [8] shows a good performance and is validated on FPGA platform. In todays science and technology, the ability of a Neural Network (NN) is to learn the dynamic behavior of nonlinear system. Authors in [9] have proposed a method based on NN for the error mitigation of ADCs. A complex digital-circuit based system carrying out an evolutionary computation algorithm is to mitigate the channel mismatch impact in TIADCs possibly employed in wideband transceivers [10]. This complex digital circuit uses the complex arithmetic functions to estimate the channel mismatches.

Channel mismatch cancellation for TIADC and linearization technique of RF component induced nonlinear are benefit from using the Deep Neural Networks (DNN) in terms of good linearization performance [11]. In DNN, various nonlinear functions are used after each convolution or fully connected computation that need to be hardware-optimized. In the transmitter chain, efficient linearization methods for wideband transmitters are highly required as well. In [12], the authors have presented an one-step solution for transmitter nonlinearity estimation and linearization control in the presence of modulator imperfections for wideband direct-conversion transmitters with neural networks. By using a two-hidden-layer feedforward neural network, a high level of transmitter linearity can be achieved. An artificial neural network can also be applied for wideband pre-distortion of efficient pico-cell power amplifiers [13].

Therefore, the objective of this work is to propose a new approach to approximate the complex arithmetic functions by using the stochastic logic combined with PWL approximation in which the coefficients are optimized to reduce the mean absolute error (MAE). The proposed approach could be applied for the channel mismatch calibration and linearization techniques based on the neural network in wideband RF transceivers. For example, a fully digital calibration of channel mismatches is pictured in Fig. 1, where the channel mismatches are estimated based on the error modeling of the complex arithmetic functions.

The remainder of this paper is organized as follows. Section II presents the proposed approach of stochastic for arithmetic functions which can be applied for wideband RF transceivers. Section III shows the ASIC implementation results and discussions. Finally, section IV concludes the paper and discusses the future research plan.

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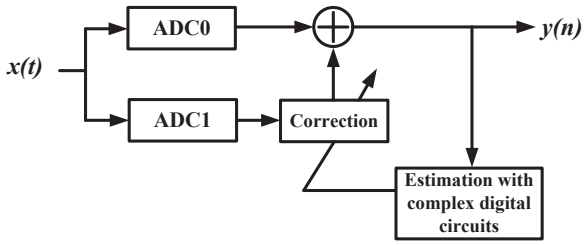

Fig. 1. All digital calibration using neural network for TIADC in the receiver part of wideband RF transceivers.

II. Proposed approach

Firstly, a complex arithmetic function $f(x)$ is approximated by using PWL approximation [7]. The domain of $x \in [\alpha, \beta]$ could be divided into s equal segments. Each segment is approximated by a linear function. To reduce the hardware complexity, the number of segments are chosen as $s = 2^k$, $(k = 1, 2, 3, 4 \cdots)$. In each segment, the function of $f(x)$ can be written as:

$$f(x) \approx a_i x + b_i, \;\; \tfrac{i}{s}(\beta - \alpha) \leq x < \tfrac{i+1}{s}(\beta - \alpha), \quad i = 0 \div s - 1. \tag{1}$$

Furthermore, the value of coefficients a_i and b_i can be described as (2), in which B represents the number of bits of a_i and b_i:

$$a_i, b_i = N \times 2^{-B} \tag{2}$$

and N is an integer number. As a result, the error in i^{th}-segment can be written as:

$$\varepsilon_i(x) = f(x) - (a_i x + b_i), \tag{3}$$

The optimized values of coefficients a_i and b_i are chosen to minimize $\varepsilon_i(x)$. The complex arithmetic functions investigated in this work include $ln(1+x)$, e^{-x}, $tanh(x)$, $sigmoid(x)$, $cos(x)$ and $sin(x)$. To balance the hardware complexity with the error, the values of $s = 8$ and $B = 8$ are chosen as well. All functions are implemented with the domain of $x \in [0, 1]$. Table I describes the optimized values of coefficients a_i and b_i achieved by an optimization algorithm performed in Matlab software. As presented in Algorithm 1, the initial value of coefficients a_i and b_i are chosen for each segment that depend on exploiting the characteristics of the complex arithmetic functions.

In PWL approximation for complex arithmetic functions of $ln(1+x)$, $tanh(x)$, $sigmoid(x)$ and $sin(x)$, the linear approximated function is represented as follows:

$$f(x) = a_i x + b_i, \;\; i = 0 \div 7. \tag{4}$$

The architecture of these functions is illustrated in Fig. 3. Two SNG blocks are implemented by 8-bit LFSRs using the polynomials of $x^8 + x + 1$ and $x^8 + x^2 + 1$ to perform the decorrelation of bit-streams. Three MSBs of the input are used to select the corresponding coefficient values in two ROMs

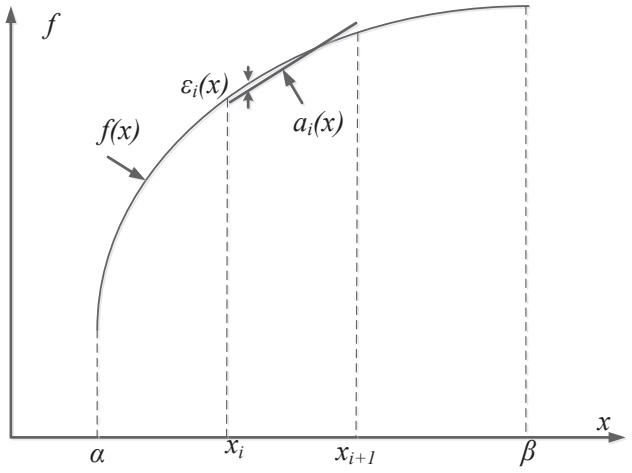

Fig. 2. Piecewise-linear (PWL) approximation for complex arithmetic functions.

	Algorithm 1: Calculating optimized values for coefficients a_i, b_i.
1:	BEGIN: Initializing arrays of a_i, b_i
2:	for i = 1: length(a) for j = 1:length(b) for k = 1:length(x) Calculating $\varepsilon_i(x)$ following (3) end end end
3:	for i = 1: length(a) for j = 1:length(b) Calculating $\varepsilon_{i\max} = \max(\varepsilon_i(x))$ end end
4:	Calculating $\min(\varepsilon_{i\max})$
5:	END: Return a_i, b_i values which produce $\min(\varepsilon_{i\max})$

denoted as ROM-A and ROM-B depending on the domain of x. It is noted that for $cos(x)$ function, the domain of coefficients is $b_i \in$ [1,2] so that the linear approximation of $cos(x)$ can be written as:

$$f(x) = (1 - a_i x) + b_i^{'}, \quad b_i^{'} \in [0, 1]. \tag{5}$$

The expression of $(1 - a_i x)$ is implemented by using NAND

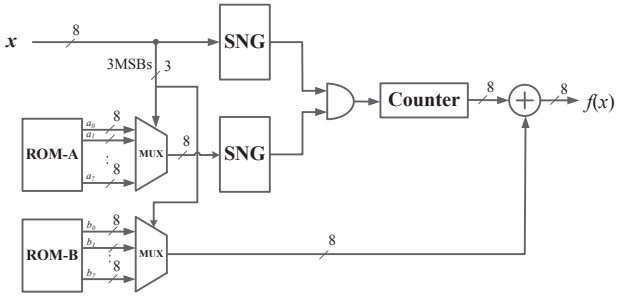

Fig. 3. The architecture of stochastic implementation of $ln(1+x)$, $tanh(x)$, $sin(x)$ and $sigmoid(x)$.

TABLE I
THE OPTIMIZED VALUES OF COEFFICIENTS a_i AND b_i ACHIEVED BY ALGORITHM 1

$\ln(1+x)$			$\tanh x$			$sigmoid(x)$		
Segment	a_i	b_i	Segment	a_i	b_i	Segment	a_i	b_i
0	243x2^{-8}	0	0	255x2^{-8}	0	0	64x2^{-8}	128x2^{-8}
1	217x2^{-8}	3x2^{-8}	1	247x2^{-8}	2x2^{-8}	1	64x2^{-8}	128x2^{-8}
2	193x2^{-8}	9x2^{-8}	2	232x2^{-8}	5x2^{-8}	2	63x2^{-8}	128x2^{-8}
3	180x2^{-8}	14x2^{-8}	3	213x2^{-8}	12x2^{-8}	3	63x2^{-8}	128x2^{-8}
4	162x2^{-8}	23x2^{-8}	4	189x2^{-8}	24x2^{-8}	4	57x2^{-8}	131x2^{-8}
5	151x2^{-8}	30x2^{-8}	5	165x2^{-8}	39x2^{-8}	5	57x2^{-8}	131x2^{-8}
6	143x2^{-8}	36x2^{-8}	6	141x2^{-8}	57x2^{-8}	6	52x2^{-8}	125x2^{-8}
7	126x2^{-8}	51x2^{-8}	7	117x2^{-8}	78x2^{-8}	7	50x2^{-8}	137x2^{-8}
$\varepsilon_{\max} = 0.0018$			$\varepsilon_{\max} = 0.0012$			$\varepsilon_{\max} = 7.1 \times 10^{-4}$		
$sinx$			$cosx$			e^{-x}		
Segment	a_i	b_i	Segment	a_i	b_i	Segment	a_i	b_i
0	255x2^{-8}	0	0	-13x2^{-8}	1	0	-234x2^{-8}	256x2^{-8}
1	254x2^{-8}	0	1	-47x2^{-8}	260x2^{-8}	1	-211x2^{-8}	252x2^{-8}
2	245x2^{-8}	2x2^{-8}	2	-79x2^{-8}	268x2^{-8}	2	-187x2^{-8}	246x2^{-8}
3	232x2^{-8}	7x2^{-8}	3	-106x2^{-8}	278x2^{-8}	3	-166x2^{-8}	238x2^{-8}
4	214x2^{-8}	16x2^{-8}	4	-138x2^{-8}	294x2^{-8}	4	-144x2^{-8}	227x2^{-8}
5	201x2^{-8}	24x2^{-8}	5	-162x2^{-8}	309x2^{-8}	5	-131x2^{-8}	219x2^{-8}
6	178x2^{-8}	41x2^{-8}	6	-186x2^{-8}	327x2^{-8}	6	-116x2^{-8}	208x2^{-8}
7	144x2^{-8}	71x2^{-8}	7	-211x2^{-8}	349x2^{-8}	7	-101x2^{-8}	195x2^{-8}
$\varepsilon_{\max} = 0.002$			$\varepsilon_{\max} = 0.0015$			$\varepsilon_{\max} = 0.0013$		

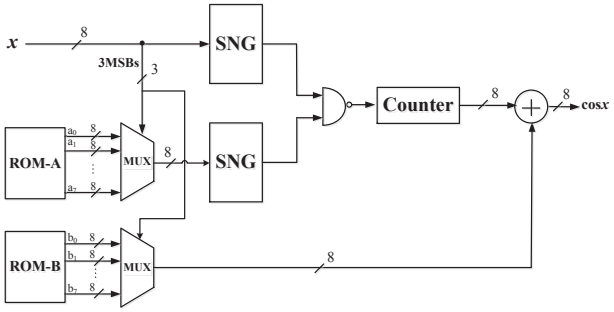

Fig. 4. The architecture of stochastic implementation of $cosx$.

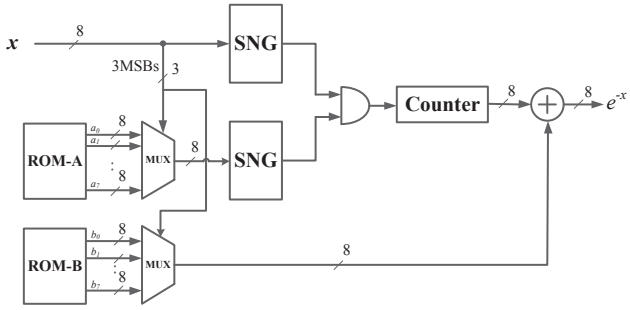

Fig. 5. The architecture of stochastic implementation of e^{-x}.

gate as mentioned in [6]. The architecture of stochastic implementation of $cos(x)$ using PWL approximation is illustrated in the Fig. 4.

In the linear approximation of e^{-x}, the domain of coefficients is $a_i \in [-1, 0]$. As a result, the absolute values of coefficients a_i are stored in the ROM-A instead of a_i. Therefore, in this architecture, the subtractor is used instead of an adder. The architecture of stochastic implementation of e^{-x} is illustrated in the Fig. 5.

III. IMPLEMENTATION RESULTS

Table II shows synthesis results of various implementations of complex functions on a 90nm CMOS library by Synopsys Design Compiler tool. The proposed designs require less hardware complexity than Horner's rule for Maclaurin expansions based implementations. The values of the critical path delay and hardware area are reduced significantly compared with [6]. Table III shows that MAE results of proposed implementations for $tanh(x)$, $sigmoid(x)$ are better than that in Horner's rule for Maclaurin expansions based, Bernstein polynomial based and finite-state-machine (FSM) based implementations as mentioned in [6]. The power consumption of the proposed approach is reduced significantly compared with Horner's rule for Maclaurin expansions based implementation as well. For a fair performance comparison in ASIC-based hardware implementation, 8-bit LFSRs are used in the proposed architecture and Maclaurin expansions based implementation [6].

Moreover, in the proposed method, the multiplier is implemented using stochastic logic. However, the addition is implemented in the binary numbers instead of stochastic computing to reduce the error. The value of coefficients of b_i was also adjusted to minimize the approximation error.

IV. CONCLUSIONS

A new approach for stochastic logic based implementation of complex arithmetic functions using PWL approximation for wideband digital transceivers was presented in this paper. The ASIC implementation and error analysis results have clarified

TABLE II
ASIC IMPLEMENTATION RESULTS OF STOCHASTIC COMPUTING USING THE PROPOSED AND MACLAURIN EXPANSIONS BASED METHODS.

Functions	Proposed approach			Horner's rule for Maclaurin expansions based method [6]			
	Area ($\times 10^3$ μm^2)	Delay (ns)	Power (μW)	Order	Area ($\times 10^3 \mu m^2$)	Delay (ns)	Power (μW)
$\ln(1+x)$	3.459	1.69	80.95	5	5.381	1.74	101.24
$\tanh x$	3.449	1.69	80.34	7	4.933	1.74	83.51
$sigmoid(x)$	3.589	1.70	97.89	5	5.350	1.74	189.17
$\sin x$	3.741	1.70	60.67	7	4.933	1.74	83.51
$\cos x$	3.746	1.70	65.87	8	5.387	1.74	103.80
e^{-x}	3.469	1.69	78.43	5	5.870	1.74	121.73

TABLE III
MAE RESULTS OF STOCHASTIC IMPLEMENTATIONS FOR DIFFERENT COMPLEX ARITHMETIC FUNCTIONS USING THE PROPOSED AND OTHER METHODS.

Functions		Proposed approach	Method in [6]			Bernstein polynomial-based method			FSM-based method
$\sin x$	Order	-	3	5	7	3	5	7	8 states
	MAE	0.0026	0.0016	0.0033	0.0034	0.0136	0.0088	0.0066	0.0025
$\cos x$	Order	-	2	4	6	2	4	6	8 states
	MAE	0.0035	0.0082	0.0025	0.0023	0.0356	0.0178	0.0120	0.0053
$\ln(1+x)$	Order	-	5	6	7	5	6	7	8 states
	MAE	0.0026	0.0141	0.0109	0.0081	0.0090	0.0076	0.0066	0.0186
$\tanh x$	Order	-	3	5	7	3	5	7	8 states
	MAE	0.0029	0.0178	0.0175	0.0140	0.0182	0.0110	0.0082	0.0351
e^{-x}	Order	-	4	5	6	4	5	6	8 states
	MAE	0.0027	0.0018	0.0008	0.0008	0.0130	0.0103	0.0086	0.0154
$sigmoid(x)$	Order	-	5			-			8 states
	MAE	0.0024	0.0046			-			0.0198

the improvement of the proposed approach. Future work will target the stochastic logic implementations for more arithmetic functions in deep neural networks using PWL approximation combined with other design techniques and an advanced ultra-low power technology for applications in wideband digital transceivers.

ACKNOWLEDGMENT

This research is funded by Vietnam National Foundation for Science and Technology Development (NAFOSTED) under grant number 102.02-2016.12.

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