

Suppression of the Self-Heating Effect in AlGa_N/Ga_N High Electron Mobility Transistor by Diamond Heat Sink Layers

Volchek V., Dao Dinh Ha, Stempitsky V.
Department of Radioengineering and Electronics
BSUIR
Minsk, Belarus
vstem@bsuir.by

Tran Tuan Trung
Le Quy Don Technical University
Hanoi, Vietnam
trung.bsuir@gmail.com

Abstract—The influence of diamond heat sink layers on the electrical characteristics of AlGa_N/Ga_N high electron mobility transistors (HEMTs) has been investigated using numerical simulation in Wachutka's thermodynamically rigorous model of lattice heating. It is shown that the diamond layers can significantly decrease device temperature, thus improving its current-voltage characteristics. Parameters of the diamond heat sink were optimized for the HEMTs on sapphire and silicon substrates.

Keywords—HEMT; self-heating; heat sink; optimization

I. INTRODUCTION

High electron mobility transistors (HEMTs) based on the AlGa_N/Ga_N heterostructure have long been contemplated to be highly promising devices for applications in power electronics, microwave systems, and sensing technologies. Due to the large electron saturation velocity along with the high breakdown voltage AlGa_N/Ga_N HEMTs can sustain substantial currents leading to very high values of the power dissipation that results in undesirable self-heating of the device. The analytical and numerical study by V. Turin and A. Balandin [1] has shown that a hot spot with a high (relatively to other regions of the transistor) temperature is formed at the drain-side gate edge as a result of the self-heating effect. Excessive heating at this region of the device causes degradation of the current-voltage characteristics. Thus, it is important to accurately simulate thermal behavior of the HEMTs in order to be able to optimize the device structure to provide better thermal stability.

Numerous approaches to reduce channel temperature have been proposed, including atomic bonding [2] or direct growth of the transistor structure on a diamond substrate [3], standard flip-chipping method to bond a heat sink [4]. Other techniques consist in integrating heat sink layers of materials with a high thermal conductivity, such as diamond [5] and graphene [6]. In this paper, we have investigated the possibility of suppressing the self-heating effect in AlGa_N/Ga_N HEMTs on sapphire and silicon substrates by applying diamond heat sink layers on top of the devices. The numerical simulation was performed using Silvaco software [7].

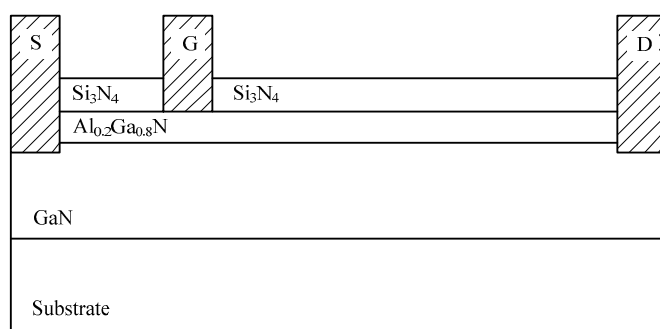


Fig. 1. Initial AlGa_N/Ga_N HEMT structure.

II. SIMULATION DETAILS

A. Structure

The two-dimensional geometry of the initial AlGa_N/Ga_N HEMT structure under consideration is schematically illustrated in Fig. 1.

The device structure consists of a 2.97 μm thick Ga_N buffer layer, a 30 nm thick Al_{0.2}Ga_{0.8}N barrier layer, and a 50 nm thick Si₃N₄ passivation layer. The substrate simulation domain thickness is 18 μm. The source-to-gate and gate-to-drain distances equal 2 μm and 8 μm, respectively, and the Schottky gate length is 1 μm. The buffer and barrier layers are n-type doped to concentrations 10¹⁵ cm⁻³ and 10¹⁷ cm⁻³, respectively.

The spontaneous and piezoelectric components of the polarization in AlGa_N are taken into account. It is assumed that the relatively thick Ga_N layer is unstrained, so it has only the spontaneous component. The two-dimensional electron gas density is calibrated to 1.07 · 10¹³ cm⁻².

B. Lattice Heat Flow Equation

The numerical simulation of the self-heating effect was carried out by implementing Wachutka's thermodynamically rigorous model of lattice heating [8]. The lattice heat flow equation which is to be solved simultaneously with the Poisson and continuity equations has the form

$$C_V(\partial T/\partial t) = \nabla(\kappa \nabla T) + H \quad (1)$$

where C_V is the heat capacitance per unit volume, T is the temperature, κ is the thermal conductivity, and H is the heat generation.

The isothermal boundary condition is set up at the bottom surface of the structure as a perfect heat sink to the room temperature $T_0 = 300$ K. The adiabatic boundary condition is applied at the top surface and the sidewalls of the device.

The model for the thermal conductivity of the materials used in the calculations is given by

$$\kappa = \kappa_0(T/T_0)^\tau \quad (2)$$

where κ_0 is the thermal conductivity at the temperature T_0 , and τ is a material dependent parameter. The values for κ_0 and τ are presented in Table I.

The parameters κ_0 and τ for $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ are calculated by linear interpolation as a function of the composition fraction.

C. Electron Mobility Model

The drift-diffusion transport model is implemented for the simulation with the Farahmand Modified Caughey Thomas mobility model [9] for electrons in the GaN channel layer. This model accounts for the impurity and temperature dependence of the electron low field mobility.

III. RESULTS

In Figs. 2 and 3 the temperature distributions along the channel of the AlGaIn/GaN HEMT without the diamond heat sink layers at different drain voltages V_d are shown for the sapphire and silicon substrates, respectively. The gate voltage is 0 V.

As follows from Figs. 2 and 3, a hot spot begins to form at the drain-side gate edge (the gate edges are indicated by the vertical lines) at high drain voltages (~ 20 V). In case of the sapphire substrate, the device peak temperature increases by 58.23 % (from 407 K to 644 K) as the drain voltage is raised from 10 V to 40 V. The maximum temperature of the transistor on the silicon substrate increases by 63.64 % (from 385 K at $V_d = 10$ V to 630 K at $V_d = 40$ V).

In Figs. 4 and 5 the electron mobility distribution along the channel of the transistor without the diamond heat sink layers at different drain voltages are shown for the sapphire and silicon substrates, respectively.

TABLE I. THERMAL CONDUCTIVITY MODEL PARAMETERS

Parameter	Material					
	Si_3N_4	Al_2O_3	Si	GaN	AlN	Diamond
κ_0 ($\text{W}\cdot\text{cm}^{-1}\cdot\text{K}^{-1}$)	0.3	0.4	1.48	1.3	2.85	22
τ	0	-1.65	-1	-0.28	-1.64	0

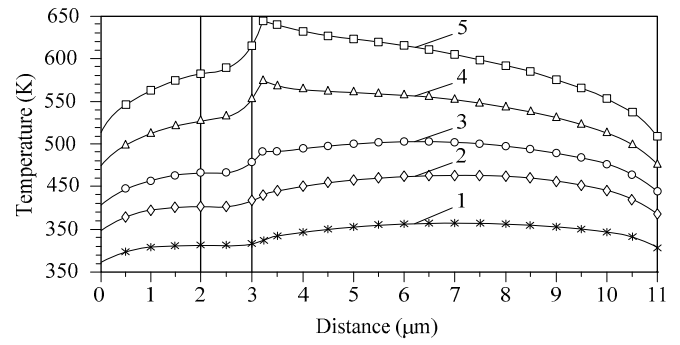


Fig. 2. Temperature distribution along the channel of the AlGaIn/GaN HEMT without the diamond heat sink layers at $V_d = 10$ V (1), 15 V (2), 20 V (3), 30 V (4), 40 V (5). The gate voltage is 0 V. The substrate material is sapphire.

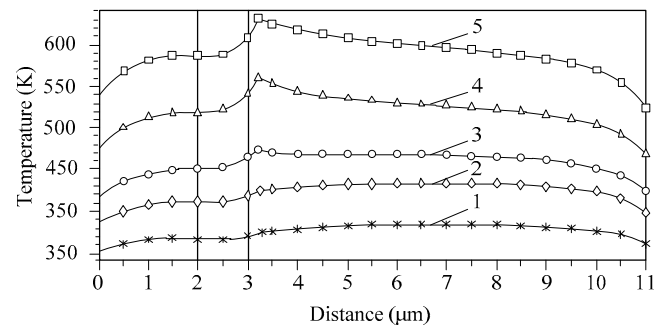


Fig. 3. Temperature distribution along the channel of the AlGaIn/GaN HEMT without the diamond heat sink layers at $V_d = 10$ V (1), 15 V (2), 20 V (3), 30 V (4), 40 V (5). The gate voltage is 0 V. The substrate material is silicon.

It is obvious from Figs. 4 and 5 that the larger the temperature a point of the device has, the less the value of the mobility the respective electrons possess. The minimum value of the electron mobility in the channel falls by 63.95 % (from $319 \text{ cm}^2/(\text{V}\cdot\text{s})$ at $V_d = 10$ V to $115 \text{ cm}^2/(\text{V}\cdot\text{s})$ at $V_d = 40$ V) if the substrate is of sapphire. In case of the silicon substrate, the mobility decrease accounts for 67.84 % (from $370 \text{ cm}^2/(\text{V}\cdot\text{s})$ at $V_d = 10$ V to $119 \text{ cm}^2/(\text{V}\cdot\text{s})$ at $V_d = 40$ V).

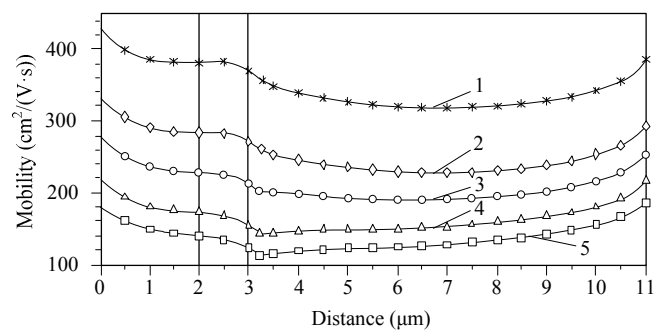


Fig. 4. Electron mobility distribution in the channel of the AlGaIn/GaN HEMT without the diamond heat sink layers at $V_d = 10$ V (1), 15 V (2), 20 V (3), 30 V (4), 40 V (5). The gate voltage is 0 V. The substrate material is sapphire.

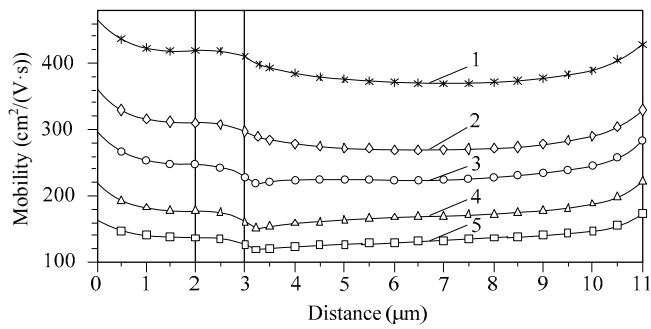


Fig. 5. Electron mobility distribution in the channel of the AlGaIn/GaN HEMT without the diamond heat sink layers at $V_d = 10$ V (1), 15 V (2), 20 V (3), 30 V (4), 40 V (5). The gate voltage is 0 V. The substrate material is silicon.

After the position of the hot spot is determined, the two diamond heat sink layers are introduced into the transistor structure: one between the source and the gate, and another between the gate and the drain. The geometry of the modified structure is illustrated in Fig. 6.

Fig. 7 shows the temperature distribution along the channel of the HEMT on the sapphire substrate without (1) and with (2) the diamond heat sink. The diamond layer thickness is chosen to be 3 μm. The drain voltage is 40 V while the gate is zero-biased. The analogous distribution for the case of the silicon substrate is shown in Fig. 8.

As follows from Figs. 7 and 8, if the substrate is of sapphire, the presence of the two 3 μm thick diamond heat sink layers allows to reduce the maximum temperature by 9.32 % (from 644 K to 584 K) at the drain voltage of 40 V. In case of the silicon substrate, the peak temperature is decreased by 6.03 % (from 630 K to 592 K). It should be noted that the heat sink reduces the temperature in the region below the gate which plays an important part in functioning of field-effect transistors.

Under the conditions indicated above the minimum value of the electron mobility increases by 20.00 % (from 115 cm²/(V·s) to 138 cm²/(V·s)) when sapphire is used as the substrate material and by 13.45 % (from 119 cm²/(V·s) to 135 cm²/(V·s)) in case of silicon.

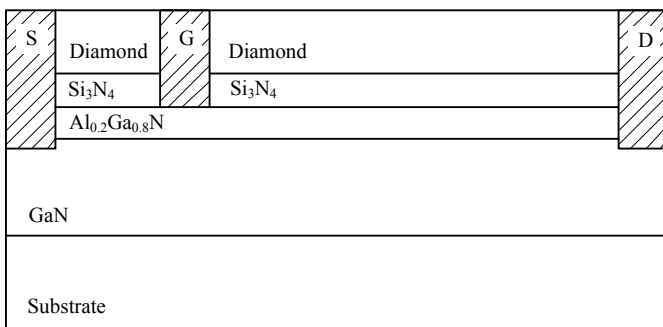


Fig. 6. AlGaIn/GaN HEMT structure with the two diamond heat sink layers.

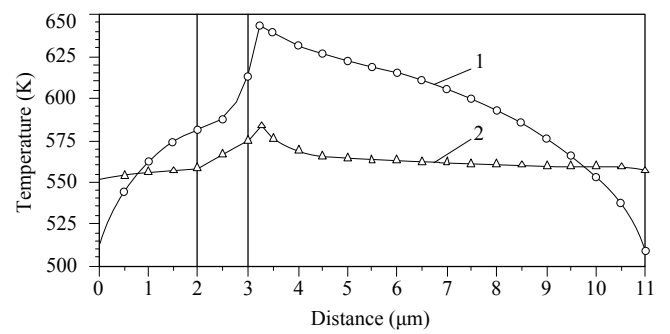


Fig. 7. Temperature distribution along the channel of the AlGaIn/GaN HEMT without (1) and with (2) the diamond heat sink layers at $V_d = 40$ V. The gate voltage is 0 V. The substrate material is sapphire.

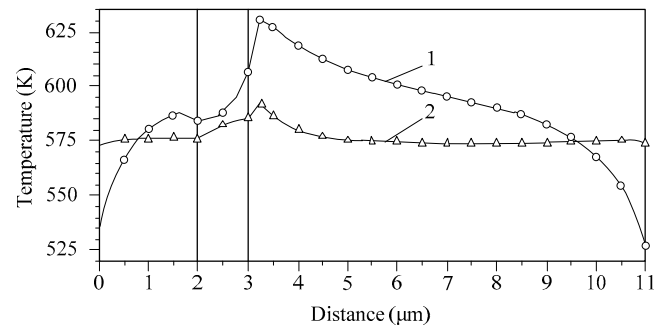


Fig. 8. Temperature distribution along the channel of the AlGaIn/GaN HEMT without (1) and with (2) the diamond heat sink layers at $V_d = 40$ V. The gate voltage is 0 V. The substrate material is silicon.

The dependence of the heat sink efficiency as a function of the diamond layer thickness at different drain voltages is plotted for the two variants of the substrate in Figs. 9 and 10. The heat sink efficiency η is given by

$$\eta = (T_0 - T_s)/T_0 \quad (3)$$

where T_0 is the maximum temperature in the HEMT structure without a heat sink, T_s is the maximum temperature in the HEMT structure with a heat sink.

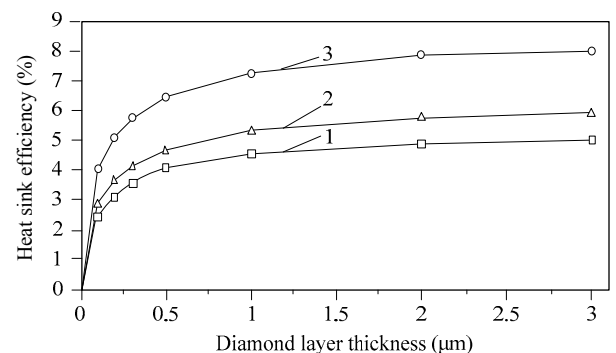


Fig. 9. Heat sink efficiency dependence on the diamond layer thickness in case of the sapphire substrate at $V_d = 10$ V (1), 25 V (2), 40 V (3). The gate is zero-biased.

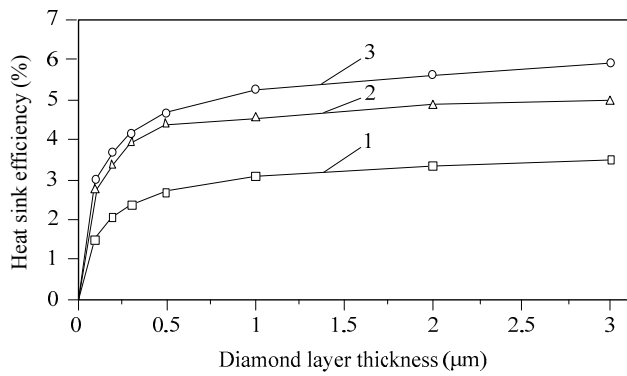


Fig. 10. Heat sink efficiency dependence on the diamond layer thickness in case of the silicon substrate at $V_d = 10$ V (1), 25 V (2), 40 V (3). The gate is zero-biased.

It follows from Figs. 9 and 10 that when the diamond layer remains relatively thin (with the thickness less ~ 1 μm) the efficiency of the heat sink displays a sharp growth but alters little with the further increase in the layer thickness. Thus, for example, the efficiency soars by 80.15 % (from 2.40 % to 4.55 %) at $V_d = 40$ V when the diamond layer thickness is changed from 0.1 μm to 1 μm for the case of the sapphire substrate. When the thickness is changed from 1 μm to 3 μm the heat sink efficiency increases only by 10.19 % (from 4.55% to 5.01 %). The corresponding values for the substrate of silicon are 78.50 % (from 2.93 % to 5.23 %) and 12.24 % (from 5.23 % to 5.87 %), respectively.

It can also be noted that the diamond heat sink efficiency in case of using the low thermal conductivity substrate (sapphire) is slightly larger than for the transistor structure on the higher thermal conductivity substrate (silicon).

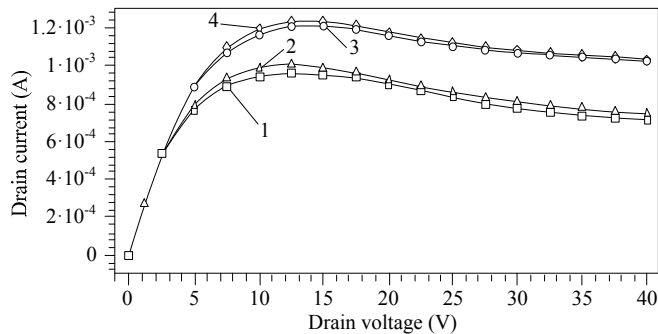


Fig. 11. Drain current versus drain voltage characteristics of the AlGaIn/GaN HEMT without (1) and with (2) the diamond heat sink layers in case of the sapphire substrate, without (3) and with (4) the diamond layers when the substrate is of silicon. The thickness of the heat sink is 3 μm. The gate is zero-biased.

The drain current versus drain voltage characteristics of the AlGaIn/GaN HEMT on the sapphire and silicon substrates without and with the diamond heat sink introduced are plotted in Fig. 11. The thickness of the diamond layers is 3 μm. The gate voltage is 0 V.

The plots in Fig. 11 show that the introduction of the two diamond heat sink layers between the source and the gate as well as between the gate and the drain improves the current-voltage characteristics of the AlGaIn/GaN HEMT structure grown on the sapphire and silicon substrates. Thus, when the 3 μm thick diamond layers are applied the maximum value of the drain current is increased by 4.99 % (from $9.62 \cdot 10^{-4}$ A to $1.01 \cdot 10^{-3}$ A) and 2.48 % (from $1.21 \cdot 10^{-3}$ A to $1.24 \cdot 10^{-3}$ A) for the sapphire and silicon substrates, respectively.

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References

- [1] V.O. Turin and A.A. Balandin, “Electrothermal simulation of the self-heating effects in GaN-based field-effect transistors,” *J. Appl. Phys.*, vol. 100, 054501-1-054501-8, 2006.
- [2] J.G. Felbinger et al, “Comparison of GaN HEMTs on diamond and SiC substrates,” *IEEE Electron Device Lett.*, vol. 28, pp. 948-950, 2007.
- [3] K. Hiram, Y. Taniyasu, and M. Kasu, “AlGaIn/GaN high-electron mobility transistors with low thermal resistance grown on single-crystal diamond (111) substrates by metalorganic vapor-phase epitaxy,” *Appl. Phys. Lett.*, vol. 98, 162112, 2011.
- [4] J. Das et al, “Improved thermal performance of AlGaIn/GaN HEMTs by an optimized flip-chip design,” *IEEE Trans. Electron Devices*, vol. 53, pp. 2696-2702, 2006.
- [5] J.E. Butler and A.V. Sumant, “The CVD of nanodiamond materials,” *Chem. Vapor Depos.*, vol. 14, pp. 145-160, 2008.
- [6] Z. Yan, G. Liu, J.M. Khan, and A.A. Balandin, “Graphene quilts for thermal management of high-power GaN transistors,” *Nature Commu.*, vol. 3, 2012.
- [7] <http://www.silvaco.com/>
- [8] G.K. Wachutka, “Rigorous thermodynamic treatment of heat generation in semiconductor device modeling,” *IEEE Trans., Computer-Aided Design*, vol. 9, pp. 1141-1149, 1990.
- [9] M. Farahmand et al, “Monte Carlo simulation of electron transport in the III-nitride wurtzite phase materials system: binaries and ternaries,” *IEEE Trans. Electron Devices*, vol. 48, pp. 535-542, 2001.