High Power Monolithic pHemt GaAs Limiter for T/R Module

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Abstract—In this paper, a high power monolithic GaAs limiter for transmit/receive module is presented. While keeping the output power below 100 mW (20 dBm), this limiter can sustain a RF input power up to 4 Watts (36 dBm). The survival input power of this limiter can get up to 10 Watts (40 dBm). This chip obtains a wide bandwidth from 7 to 21 GHz. Within this band, the chip has the insertion loss lower than 2.3 dB and achieves only 1 dB insertion loss in the X-Band from 7 GHz to 12 GHz.

Index Terms — X-Band; Ku-Band; Limiter; GaAs; transmit/receive module; monolithic; high power; Watt level; pHempt.

I. INTRODUCTION

A X-band Transmit/Receive Module (T/R Module) is often used in a high power phase-array radar system. As can be seen in Fig.1, It comprises both transmitter and receiver front-ends of a radar system, in which the output power of the transmitter is much higher than the input power of the receiver. Therefore, a limiter is placed ahead of the low noise amplifier (LNA) to protect receiver front-end against high radio frequency (RF) power leaking from transmitter front-end. High power limiters, which can sustain at watt-levels RF power, are often produced using specialized processes such as PIN diode on Silicon or GaAs substrates [1, 2, 3]. These processes provide high power, broadband and low loss limiters. However, thousands of T/R modules are used in a phase-array system and in some cases, it is preferable to integrate monolithically limiters to LNAs (or receiver systems) [4, 5] due to extremely size constraint. For that reason, using standard processes, such as GaAs pHemt [6, 7] and BiCMOS [8], is preferable and provides more cost effective solution. The work in [7] has the same frequency band with this work but used the 0.5μm gate length process which has higher breakdown voltage. However, it ended up with lower measured withstand power and double the size. Besides, its large parasitic capacitance resulted narrower operation bandwidth and more insertion loss.

Research works on limiters using standard GaAs pHemt technology have been very limited today. The basic limiter circuit shown in Fig. 1b has very low power sustainability because of low breakdown voltage. In this paper, a design of high power broadband monolithic limiter on commercial 0.15um pHemt GaAs process from Win Semiconductors [9] is proposed. The breakdown voltage is increased by stacking multiple diodes and therefore, increases the withstand power. A wide bandwidth of 7 GHz to 21 GHz is achieved by applying distributed structure, in which parasitic capacitance of diodes is absorbed by distributed transmission line. The voltage and current swings at each stage are carefully calculated to

keep the output power level below 100 mW. The limiter have a low insertion loss of 1 dB for the frequencies from 7 GHz to 12 GHz. It can withstand up to 10 W input power which is the highest survival input power for a limiter on a standard commercial pHemt GaAs process that has ever been published.
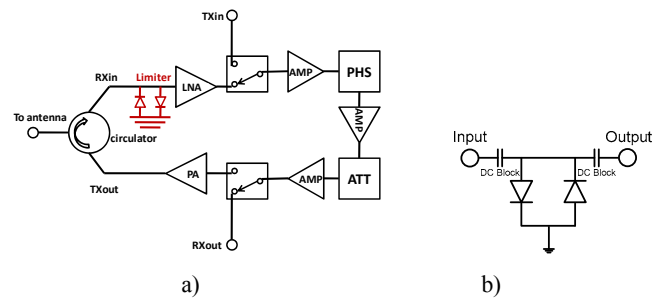

Fig. 1. a) Block diagram of a T/R Module b) Basic limiter circuit

II. LIMITER DESIGN
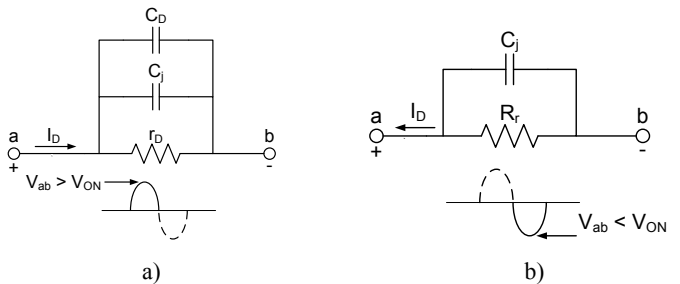
A. The diode model

Fig. 2. The AC equivalent circuits of a diode a) Forward bias b) Reverse bias

Fig. 2 shows the AC signal equivalent circuits of a diode. V_{ab} is the voltage across the diode and V_{ON} is the turn-on voltage of the diode. On the positive half circle of the input signal, the diode is in forward biased mode when $V_{ab} > V_{ON}$. The AC diode model of this mode is shown in Fig. 2a. In this model, the junction capacitance C_j is parallel with C_D, the diffusion capacitance due to charge storage. These parasitic capacitances will cause a lot of problems for high frequency operation of a diode. The forward biased resistance r_D is also a function of frequency. Fig. 3a presents the measured forward biased IV-curve of a 4x40 um diode in 0.15um pHemt GaAs process of WIN Semiconductors [9]. The turn-on voltage V_{ON} is about 0.8

V for 1 mA current. At this point, the r_D is 37 Ohm. If we cascade 3 diodes in series, the total resistance will be R = 111 Ohm. When the limiting process starts at about 15 dBm root mean square (rms) input power of sinusoidal signals, according to the equation:

$$P_{rms} = \frac{V_{Pk}^2}{2R} \ (W) \qquad (1)$$

the peak voltage (V_{pk}) at input of 3 diodes in series will be 2.64 V, that matches the necessary voltage to turn-on the 3 diodes. Therefore, we need to cascade 3 diodes in series to limit output power level under about 15 dBm.
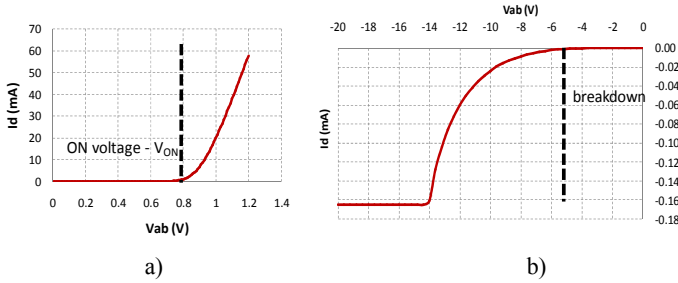

Fig. 3. The IV-Curve of the 4x40 um diode a) Forward bias b) Reverse bias

On the negative half circle of the input signal, the diode is in reverse biased mode since $V_{ab} < V_{ON}$. This introduces a junction capacitance (C_j) in parallel with the very large reverse biased resistance (R_r) as shown in Fig. 2b. Since the maximal reverse biased voltage that can be applied to the diode is limited by the breakdown of the p-n junction, it will characterize the survival power of the diode. As shown in Fig. 3b, the reverse breakdown voltage of this diode is about 5.5 V. Hence, the withstand power of the circuit is at the level where the voltage swings across each diode must not exceed 5.5 V.
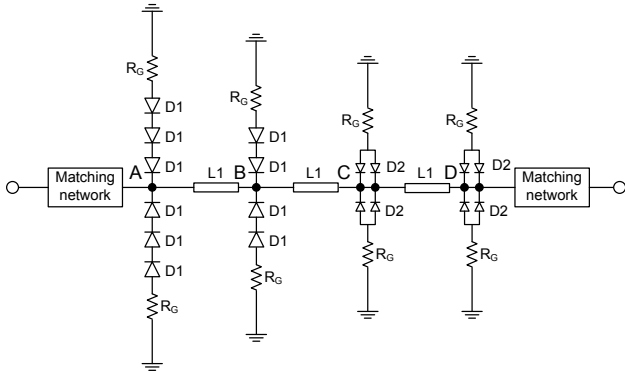

Fig. 4. Limiter schematic diagram

B. Limiter design

Fig. 4 presents the schematic diagram of the proposed limiter. The size of the diode also determines the power handling capability of the diode. A large diode can conduct more current and therefore, suppress output power better. However, it has more capacitance and less bandwidth. In this work, the diodes D1 at point A and B are 4 x 40 um and the diodes D2 at point C and D are 2 x 40 um to optimize for the

matching bandwidth. Since we want a wide bandwidth and high survival power while limiting low output power, the distributed structure is applied [10]. With smaller size, the diodes at points C and D have ON voltage of 1 V for 1 mA current and ON resistance of 42 Ohm. As a result, they are predicted to turn on first at the rms input power about 11 dBm. Then, when the input power goes up, the diodes at point B and A will be turned on in turns. That distributes the power through multiple stages and therefore, increases the power handling of the limiter. Besides, with the distributed structure, the parasitic capacitances of diodes will be absorbed by the distributed transmission lines L1. That enhances the matching bandwidth of the limiter. The small 3 Ohm resistors R_G are added to each stage to absorb the leaking RF power.
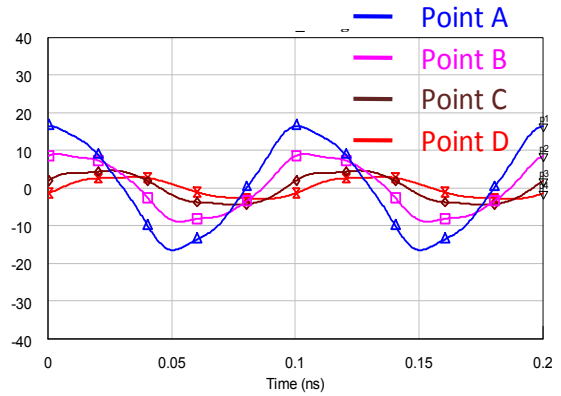

Fig. 5. Voltage swings at point A, B, C, D when the input power is 40 dBm

Fig. 5 is the simulated voltage swings at points A, B, C, D respectively when the input power is 40 dBm or 10 Watts at 10 GHz. As can be seen, the peak voltage at point A is about 16.4 V, below 10 V at point B and below 5 V at point C and D. Hence, with a breakdown voltage of 5.5 V for each diode, the survival power of 10 Watts is predicted for this limiter.

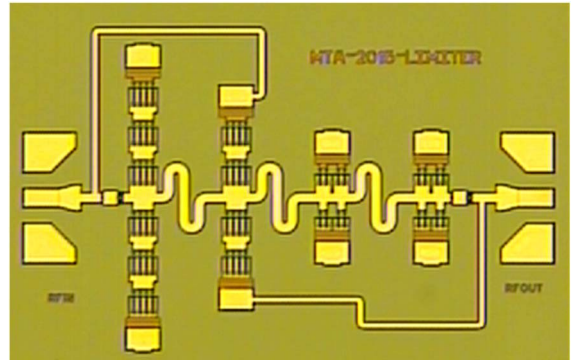### III. THE LIMITER PROTOTYPE AND MEASUREMENT RESULTS

Fig. 6. The photo of limiter

The photo of the fabricated limiter chip is presented in Fig. 6. The size of the whole layout is 1.4 mm x 0.83 mm including RF probe pads for on-wafer measurement.The small signal performance of the limiter was measured on a Cascade

Microtech probe station with an Agilent E8364 2-port network analyzer. The probes were calibrated by using Thru-Reflect-Line calibration on a Picoprobe CS-5 substrate. Fig. 7 shows the measured and simulated S-parameters of the limiter.
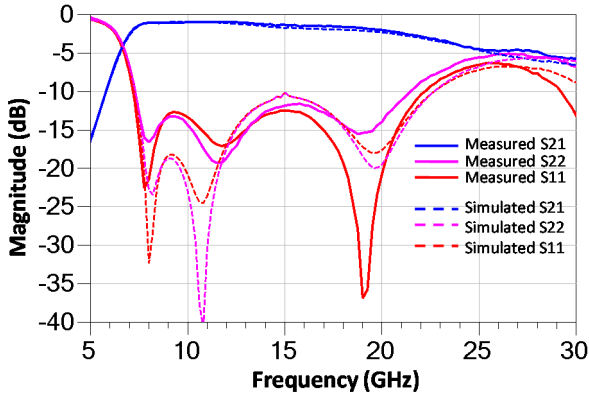

Fig. 7. Measured and simulated S-parameters of the limiter

As shown in Fig. 7, the measured results match with what we simulate. The limiter has the measured input and output return loss of better than 10 dB from 7 GHz to 21 GHz. The measured insertion loss is better than 1 dB in X-Band (from 8 GHz to 12 GHz) and decreases gradually to 2.3 dB at 21 GHz.

The large signal performance of this limiter was performed by N9030A PXA Signal Analyzer. To measure the limiter at its breakdown region, a HUGHES 1177H X/Ku band travelling wave tube amplifier is employed to provide up to 10 Watts power from 8 GHz to 18 GHz. A CW signal was used to feed the limiter. Fig.8 shows the measured output power versus frequency when the limiter is driven by 36 dBm input power. It is shown that the limiter is able to limit the output power below 20 dBm over a wide bandwidth and this performance gets better when the frequency goes up.
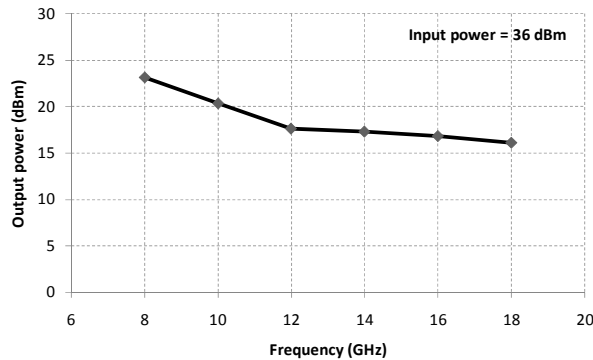

Fig. 8. Measured output power versus frequency for 36 dBm input power

The measured Pin versus Pout performance at 10 GHz is shown in Fig. 9. The diodes in the limiter are turn on as the input power gets to 15 dBm and help to limit the output power under 30 dBm up to 36 dBm input power. The survival input power of the limiter can get up to 40 dBm with CW signal when the breakdown of the diodes occurs.
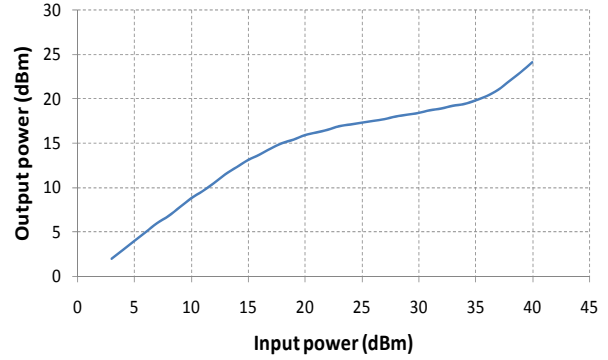

Fig. 9. Measured input power versus output power at 10 GHz

Table I summarizes performance and compares this work with some previously published X-Band MMIC Limiters at X-band. As being seen, this limiter is although designed using a standard commercial process but it still has competed performance with the ones designed using specialized processes (ex. VPIN GaAs) and its size is very compact.

IV. CONCLUSION

A compact, wideband, high power limiter for radar T/R module at X-Band has been presented. This limiter is designed on 0.15 um pHemt GaAs standard process and achieves an excellent performance. The measured results show that the proposed limiteris able to limit the output power under 20 dBm and withstand the input power up to 40 dBm. The return loss is better than 10 dB from 7 GHz to 21 GHz and the insertion loss is 1 dB in X-Band.

TABLE I.   LIMITER PERFORMANCE SUMMARY AND COMPARISON

References	This work	[7]	[11]	[12]
Freq. (GHz)	7-21	6-14	3 - 28	6-15
Insertion loss (dB)	1	1.4	0.38	0.5
Limited output power (dBm)	20	20	17	18
Withstand input power (W) (CW signal)	10	8	4	10
Size (mm^2)	1.162	2.4	1.038	4
Process	0.15um pHemt GaAs	0.5um pHemt GaAs	VPIN GaAs	VPIN GaAs

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