Hardware Implementation of Cyclic Codes Error Correction on FPGA

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***Abstract*—This paper designs and implements a codec system using the Cyclic code on FPGA. The encoding system was based on the principle of dividing circuits and the decoding system was based on the principle of the Meggitt decoder. This work proposes the look-up table (LUT) method for the decoding system. The implementation results from FPGA show that the proposed decoding method has exactly resulted. In addition, the proposed cyclic decoder core using the look-up table method has lower resource and number of cycles compared to the cyclic decoder core using the Meggitt method.**

Keywords—encode; decode; fpga; cyclic

I. INTRODUCTION

Recently, the Cyclic code has played a significant role in high speed Networks, namely 10G Ethernet, 100 G Ethernet [1]. Figure 1 presents a part of 40/100 GbE PHY architecture with a forward error correction (FEC) sublayer[2]. The Cyclic codes are used in FEC such as the Meggitt decoder[3],[4] , error-trapping decoding [5]. The [5] uses Meggitt decoding rule can be designed with simple combination logic circuits.

The hypothesis of this paper is to show that the cyclic decoder LUT method is more efficient than the Meggitt method. This work is organized as follows: Section II describes the theory of encoding and decoding cyclic code, section III presents the encoding and decoding designs, and Section IV shows the implementation results. Finally, section V concludes the paper.

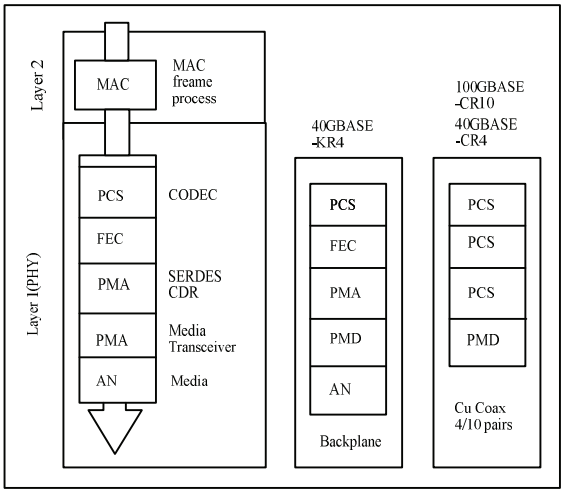

Figure 1. A part of 40/100GbE PHY Architecture.

I. BACKGROUND OF CYCLIC ENCODER AND DECODER

A. *Encoding cyclic code for (7,3,1) code*

The generator polynomial of the (7,3,1) cyclic :

$g(x) = x^4 + x^2 + x + 1$

We adopt the encoding circuit based on g(x) from the study of Roberto Togneri [5]:

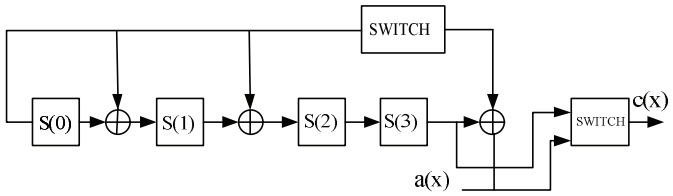

Figure 2. The encoding circuit for the (7,3,1) cyclic code

Encoding formula of cyclic codes:

$c(x) = x^{n-k}.a(x) + \text{rem}\{x^{n-k}.a(x)/g(x)\}$

a(x) is the information code polynomial, c(x) is the codeword polynomial. The Figure 3 shows the (7,3,1) cyclic encoding circuit. The feedback register is based on the coefficients of the generator polynomial. The principle of the encoding circuit was described in the research of Y .Li [3]. The detail implementation of this circuit will be presented in the Section III.

B. *Meggitt decoder theory for (7,3,1) cyclic code*

A general decoder for (7,3,1) cyclic code is shown in Figure 3.

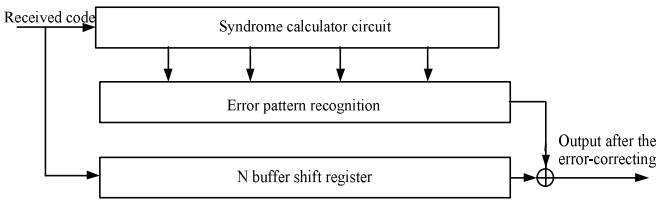

Figure 3. The operational principle of the Meggitt decoder

It consists of three major parts:

- A syndrome register [6]

- An error pattern detector

- A buffer register

The decoder based on error pattern recognition is defined by Meggitt decoder. The operational principle of the Meggitt decoder is described in previous study conducted by Y .Li [3].

Let r = (r_0, r_1,…r_{n-1}) be the received vector. The received polynomial r(x) is shifted into the register with initial state set to 0. The syndrome can be accomplished with a division circuit as illustrated in Figure 4[2]:

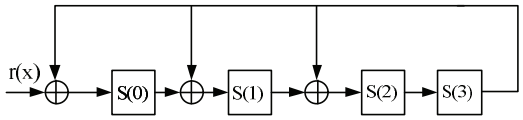

Figure 4. The syndrome calculator

If the syndrome s = (0000), the received codeword is correct. In contrast, if s # (0000), this state is set as the initial state of the spontaneous calculator detecting the position of the error codes in Figure 5.

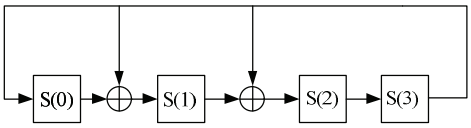

Figure 5. The spontaneous calculator

C. LUT decoding method

This study supports the use of Look Up Table method decoding. The idea is based on the relationship between the syndrome and the error pattern, as illustrated in table I[7] . The decoding structure using LUT method is shown in Figure 6.

TABLE I. THE BIT ERROR PATTERN PRODUCED THE SYNDROME

Error bit $e_6e_5e_4e_3e_2e_1e_0$	Syndrome $s_0s_1s_2s_3$
1000000	1011
0100000	1110
0010000	0111
0001000	1000
0000100	0100
0000010	0010
0000001	0001

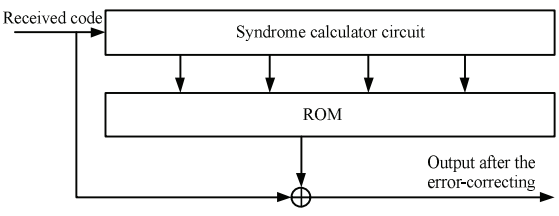

Figure 6. The architecture of (7,3,1) Cyclic codes decoding using LUT method.

II. CYCLIC ENCODER AND DECODER DESIGN

Principle of dividing circuit in section 2 used to design (7,3,1) Cyclic codes encoding is shown in figure 7.

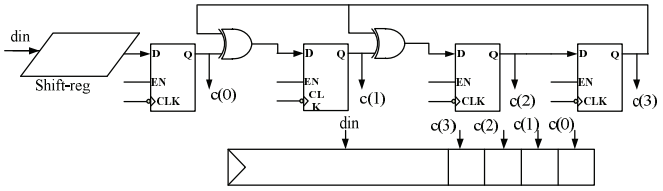

Figure 7. The architecture of (7,3,1) cyclic codes encoding.

The architecture of (7,3,1) Cyclic codes decoding using Meggitt method is presented in figure 8.

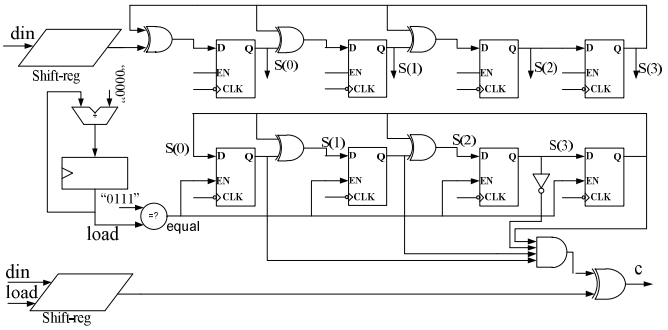

Figure 8. The architecture of (7,3,1) cyclic codes decoding using Meggitt method.

This work proposes the architecture of (7,3,1) Cyclic codes decoding using LUT method shown in figure 9. In this method, the ROM is calculated including the constants as presented Table I.

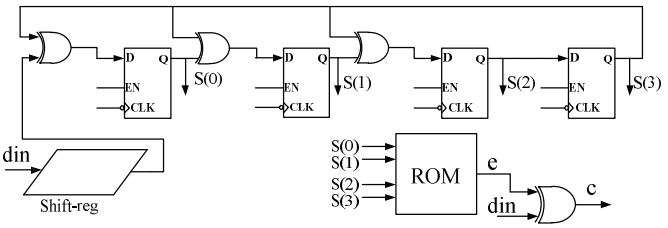

Figure 9. The architecture of (7,3,1) Cyclic codes decoding using LUT method.

III. IMPLEMENTATION RESULTS

The Cyclic encoder and decoder core is implemented the simulation model for Cyclic encoder and decoder core with VHDL code [8], [9], simulation in Modelsim tool. Figure 10 shows the input generation block generates the input vector values for Cyclic encoder and decoder core verification. Figure 11 presents the simulation result in Modelsim tool.

The FPGA implementation results are shown in Table II and Table III in which Cyclic encoder core area and number of cycles is lower than Cyclic decoder core. Moreover, The proposed Cylcic decoder core using LUT method has resources and number of cycles that are lower than cyclic decoder core using Meggitt method though the speed was found lower.

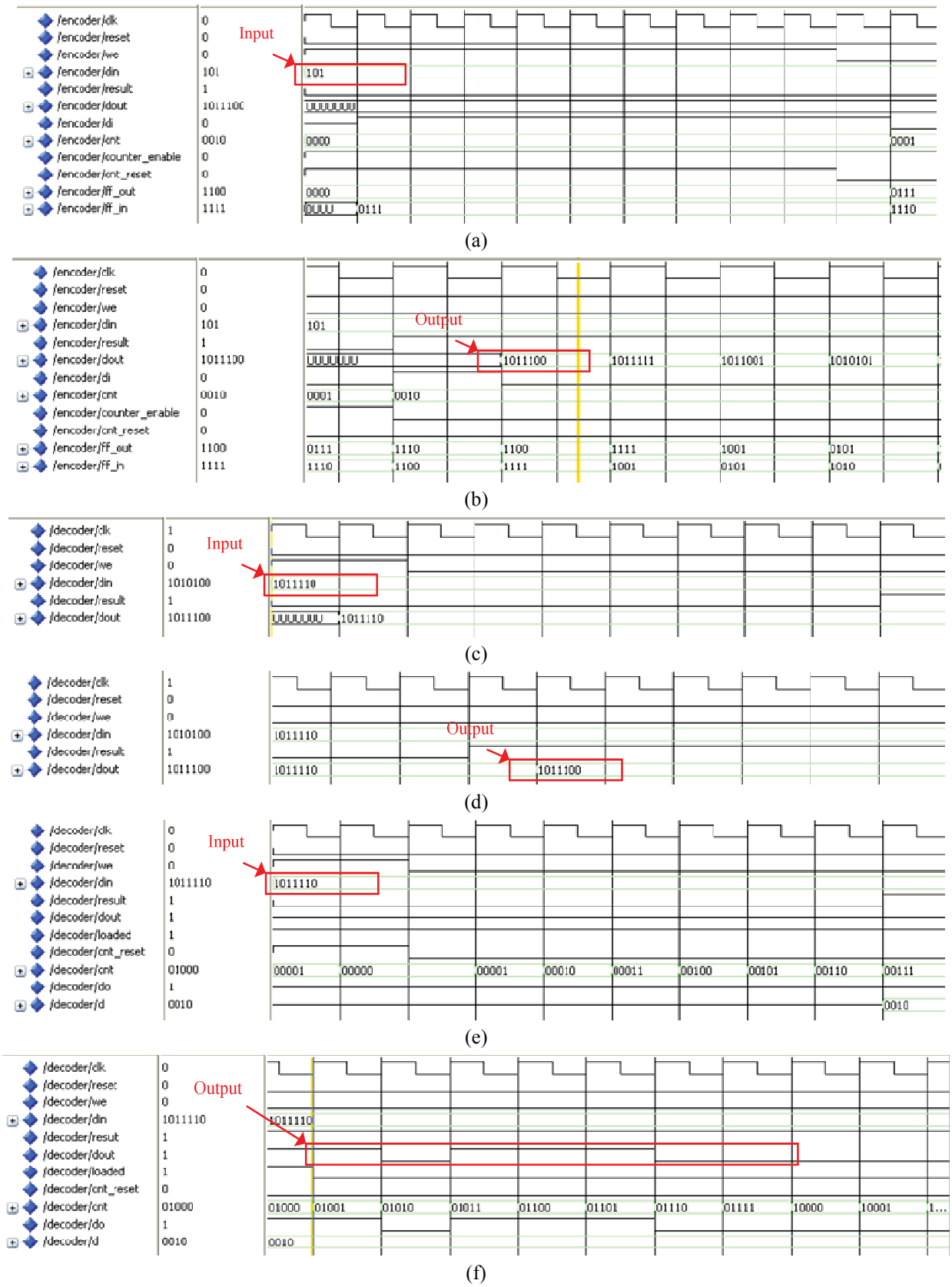

Figure 11. Simulation results in Modelsim tool (a) Data input for encoder; (b) Data output for encoder; (c) Data input for decoder LUT method; (d) Data output for decoder LUT method; (e) Data input for decoder Meggitt method; (f) Data output for decoder Meggitt method.

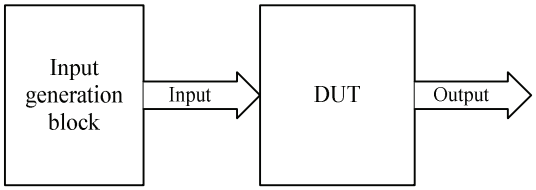

Figure 10. The simulation model for encoder and decoder of Cyclic codes.

TABLE II. IMPLEMENTATION RESULTS OF CYCLIC ENCODER ON XILINX SPARTAN-3E FPGA.

	(7,3,1)	(15,11,1)	(31,26,1)
Number of Slices	11	21	40
Number of Slice Flip Flops	18	34	67
Number of 4 input LUTs	14	21	39
Speed	302	279	216
Cycles	3	11	26

TABLE III. IMPLEMENTATION RESULTS OF CYCLIC DECODER ON XILINX SPARTAN-3E FPGA.

	LUT (7,3)	Meggitt (7,3)	LUT (15,11)	Meggitt (15,11)	LUT (31,26)	Meggitt (31,26)
Number of Slices	16	20	26	30	50	52
Number of Slice Flip Flops	21	30	38	48	72	84
Number of 4 input LUTs	31	35	47	52	92	94
Speed	264	274	247	274	188	235
Number of Cycles	8	16	16	32	32	64

IV. CONCLUSIONS

This paper has presented a method to implement Cyclic codes encode and decode on FPGA. The implementation results in FPGA show that by using LUT method, the Cyclic decoder area and number of cycles can be reduced significantly compared to Meggitt method. In the future, we will optimize the power consumption and area for the proposed Cyclic decoder core and apply it for a high speed protocol application.

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