High Dynamic Range X-Band MMIC VGLNA for Transmit/Receive Module

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***Abstract*— In this paper, a monolithic variable gain low noise amplifier (VGLNA) for transmit/receive module is presented. The voltage controlled attenuator (VCA) in the VGLNA helps to control the gain of the LNA for 20 dB range. This core-chip achieves a high dynamic range with the measured minimum Noise Figure (NF) of 1.2 dB and OIP3 of 29 dBm at 9 GHz. The operating bandwidth of this chip is from 7.5 GHz to 10.5 GHz. Within this band, the chip has the NF lower than 1.5 dB, the gain higher than 24 dB and the OIP3 better than 25 dBm. The 1 dB compression point is 14 dBm at the output.**

Keywords—Low noise amplifier; Voltage controlled attenuator; GaAs; transmit/receive module; X-Band

I. INTRODUCTION

Transmit/Receive Module (T/R Module) is an important element in a radar system. It comprises both transmitting and receiving radio frequency signal function and determines crucial parameters of a radar. Fig.1 shows the block diagram of a T/R module. In this diagram, low noise amplifier (LNA) is the first component in the receiver chain of the T/R module ;therefore, has significant effect on noise figure (NF), gain, bandwidth (BW), dynamic range, spectral purity...of the system. Hence, a low noise, wideband, high gain, high power and linear LNA is highly required for a high quality radar system. Besides, depending on the power level of the received signal, the gain of a LNA also needs to be controlled automatically to have desired power levels at the inputs of succeeded components in the system.

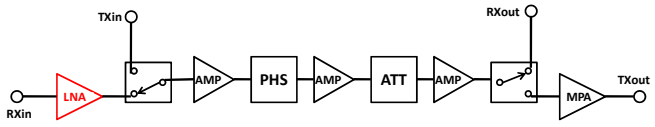

Fig. 1. Block diagram of a T/R Module

Recently, there are numerous publications on X-band LNA as the X-band radar system becomes a popular topic. However, not many of these LNAs have controllable power gain ability. [1, 2, 3, 4] are just a few of them that propose variable gain low noise amplifier (VGLNA) at X-Band. These circuits were designed on silicon substrates and provide wide bandwidth with small dimension. However, their noise figures are larger than 2 dB [1, 2, 3] and their OIP3s are smaller than 19 dBm [1, 2, 3, 4], that makes these circuits difficult to integrate into a system required high dynamic range. On the other hand, circuits designed on Gallium Arsenide (GaAs) substrates can provide low noise, higher power, reliability and hence, higher dynamic range. In this paper, a high dynamic range LNA with integrated VCA for variable gain is proposed. This circuit is designed on 0.15um pHEMT GaAs technology from Win Semiconductors [5] and achieves the operation bandwidth from 7.5 GHz to 10.5 GHz. In this frequency band, the chip has the noise figure lower than 1.5 dB, the gain higher than 24 dB and the OIP3 better than 25 dBm. The minimum noise figure is 1.2 dB at 9 GHz, while the OIP3 at this frequency is 30 dBm. The 1 dB compression point of this circuit is 14 dBm at the output. To the knowledge of the authors, this is the highest OIP3 and the lowest noise figure X-Band VGLNA that has been published in the literatures.

II. LNA DESIGN

A. LNA topology

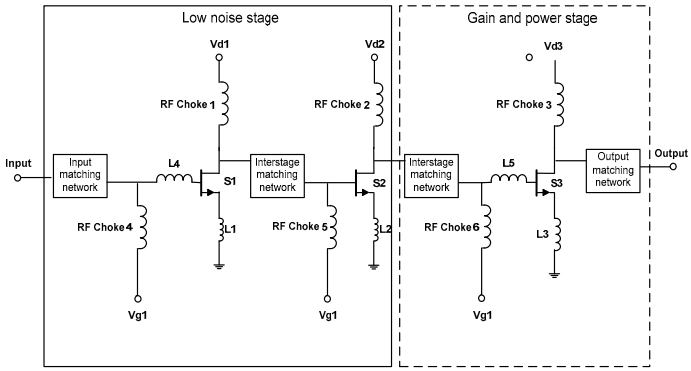

Fig. 2. LNA Topology

Fig.2 presents the designed LNA topology. This LNA consists of three amplifying stages in order to produce the desired gain. The first two transistor stages are designed to have a low noise figure, whereas the last stage is optimized for gain, output power, circuit stability and linearity. Choke inductors are used at all DC bias paths to prevent signal leakage. The LNA utilizes inductive source degeneration technique with inductors L_1, L_2 connecting to the sources of the two first common source amplifiers S_1, S_2 in order to achieve good return loss and low noise at the same time over a wide bandwidth. The small inductor L_3 connects with the source of the transistor S_3 to reduce the third order intermodulation (IM3) of the circuit and ease the output matching.

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B. Design for low noise figure

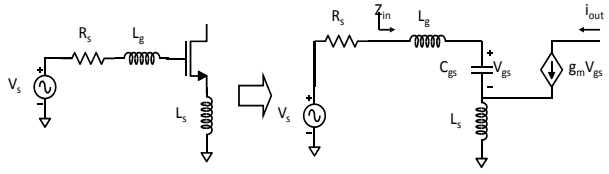

Fig. 3. Inductive source degeneration topology and its small signal equivalent circuit.

As being discussed in the previous session, the first two stages are designed to obtain low noise figure. [6] shows that good return loss and noise performance can be achieved simultaneously by applying inductive source degeneration incorporating with optimal impedance matching at the input. The schematic of inductive source degeneration transistor and its small signal equivalent circuit are shown in Fig.3. The input impedance Z_{in} of this circuit is calculated [6]:

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \qquad (1)$$

And the noise figure can be given as:

$$NF\big|_{\omega\approx\omega_0} = 1 + \gamma\frac{4(g_m L_s)^2}{R_s g_m}\frac{1}{C_{gs}(L_g + L_s)} = 1 + \frac{4\gamma L_s}{L_g + L_s} \qquad (2)$$

where γ is empirical constant and equals 2/3 for long channel. (1) and (2) shows that good return loss and noise matching can be obtained simultaneously by having large L_g and choosing appropriate L_s. However, L_s should be selected carefully, since available gain is reduced with large L_s [7]. In the first two stages of this design, the source degeneration inductor L_1 and L_2 are selected about 0.5 nH. Besides, a minimum noise factor, F_{min}, can be achieved when a particular reflection coefficient, $\Gamma_s = \Gamma_{opt}$, is presented to the input [6]. That means L_g and the input matching network should be designed to meet the optimal impedance at the input. Therefore, after selecting L_s, the impedance of $\Gamma_s = \Gamma_{opt}$ is searched by doing source-pull simulation at the gate of a transistor connected with source degeneration inductor L_s. Fig.4 shows the impedance contours at the input for the lowest noise figures. In the ideal lossless condition, the minimum noise figure of the transistor in this design is about 0.6 dB at 95 + j82.35 Ohm. Therefore, the input matching network including L_4 is optimized to not only deliver an impedance closed to this optimal impedance, but also provide a good return loss at the input. The gate width of the transistors of the first and second stage is 150 µm. The transistors are biased at $V_{d1} = V_{d2} = 2$ V and $V_{g1} = V_{g2} = -0.8$ V with the drain current $I_{d1} = I_{d2} = 22$ mA.

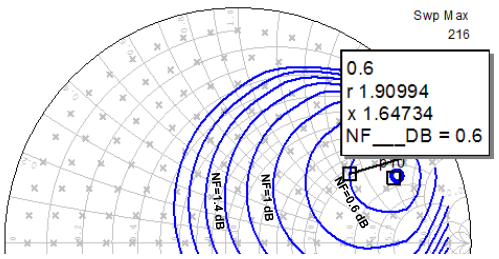

Fig. 4. Source-pull simulation: input impedance contours versus Noise Figure (dB) (Ref. Impedance: 50 Ohm)

C. Design for high linearity

Unlike the first two stages, the third stage of this LNA is designed for gain, output power and linearity. [8] and [9] show the dependence of the third order intermodulation distortion (IMD3) of a common-source amplifier when the two tones input signal $v_{in}=V[\cos(\omega_1 t) + \cos(\omega_2 t)]$ is applied:

$$\left|IMD3(2\omega_1 - \omega_2)\right| \propto \left|1 + j\omega C_{gs} Z_g(\omega) + j\omega C_{gs} Z_s(\omega)\right| \qquad (3)$$

where ω_1 and ω_2 are angle frequencies of the two tone input signals, ω is center angle frequency, $Z_g(\omega)$ and $Z_s(\omega)$ are the impedances at the gate and source of a common-source amplifier stage, respectively. If inductance is at this gate or this source as in Fig.3, $Z_g(\omega) = j\omega L_g$ or $Z_s(\omega) = j\omega L_s$, the terms $j\omega C_{gs} Z_g(\omega)$ or $j\omega C_{gs} Z_s(\omega)$ will be negative and therefore, the IMD3 will decrease when the inductance L_g or L_s increases. Hence, at the third stage, two inductors L_3 and L_5 are used at the source and the gate to enhance the linearity. Again, the inductor at the source L_3 is very small to avoid gain reduction. The output matching network is designed to balance between a good wideband S_{22}, flat gain and high output power. The total gate width of transistor in the third stage is also 150 µm. The drain voltage at this stage is biased 5V, higher than at the first two stages (2V), to get high output power.

D. LNA simulation results

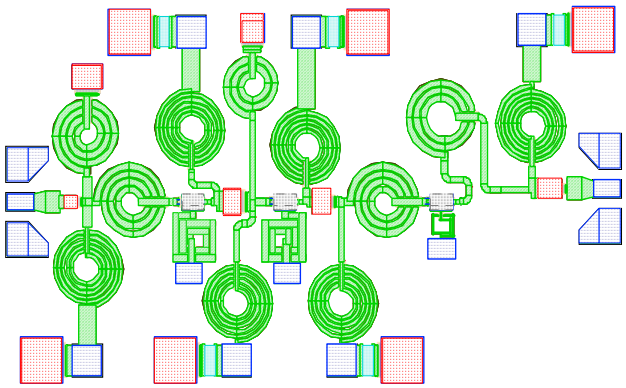

Fig. 5. Designed LNA's layout

Fig.5 is the designed layout of the LNA. The dimension is 2.1mm x 1.2mm including DC bias pads and RF probing pads. The coupling effects and parasitic of the layout are predicted by electromagnetic simulator AXIEM of Microwave Office AWR [10]. The performance of the LNA is also predicted by using AWR. The simulated S-parameters, noise figure and OIP3 of this LNA is presented in Fig.6. According to the simulation results, the LNA can achieve the minimum noise figure of 1.2 dB at 10 GHz, the gain about 29 dB from 6 GHz to 12 GHz. The OIP3 is simulated by applying -20 dBm two tones signal at the input, these two tones are separated by 10 MHz to each other. The LNA has higher than 25 dBm OIP3 for the frequencies from 5 GHz to 14 GHz and achieves the maximum OIP3 of 31 dBm at 9.5 GHz.

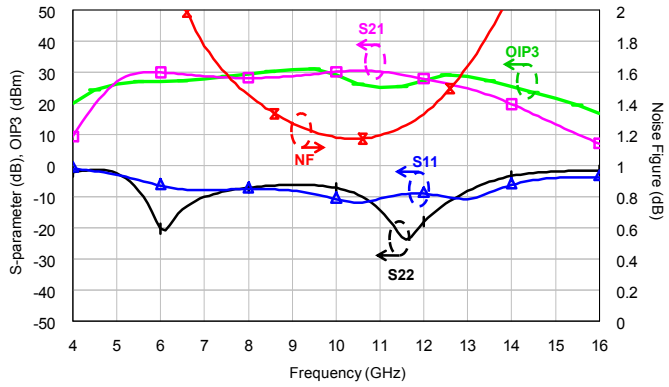

Fig. 6. Simulated performance of the proposed LNA

III. VCA DESIGN

A. VCA topology

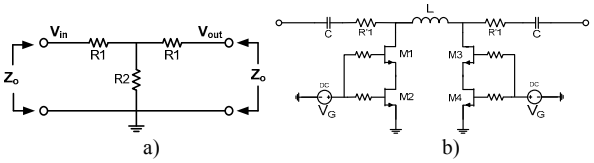

Fig. 7. a) Tee attenuator b) Proposed VCA topology

The design of VCA is inspired from the "Tee attenuator" topology which is shown in Fig.7a. The attenuation of the "Tee attenuator" circuit is fixed and determined by the resistors R_1, R_2 and the termination impedance Z_o [11]. If we can change the values of these resistors, we can vary the attenuation caused by the circuit. A FET transistor can be used as a variable resistor when it is biased in triode region. Fig.8a shows the IV-curve of a 4x75 µm gate width transistor of 0.15um GaAs pHemt process and Fig.8b is its equivalent circuit when biased in triode region. In this figure, the resistance of this transistor $r_{DS} = dV_{DS}/dI_D$ can be varied by changing the gate voltage V_{gs}. Hence, we can vary the attenuation of a attenuator circuit by replacing its resistors by FETs and biasing properly. However, the parasitic capacitance C_{DS} of a FET is also varied with V_{gs} and operation frequencies. This will cause a lot of difficulties in impedance matching at the input and output when designing a VCA.

From the above analysis, the topology of proposed VCA is created as Fig.7b. In this structure, the two resistors having the same value R'1 are replaced for the two resistors R1 in Fig.7a. Although resistors cause more loss, the authors still tried to avoid using FETs for these positions, because they will decrease the linearity of the circuit and make the circuit more complicated with added control voltage. Total resistance of the transistors M_1, M_2, M_3, M_4 represents for resistor R_2. All transistors are biased with the same gate voltage V_G. This resistance can be changed by changing V_G. The transistor gate width also affects its resistance, the smaller the gate width, the less resistance and vice versa. In this design, the gate width of each transistor is 300 µm. Inductors L is placed between M_1 and M_3 to compensate for the parasitic capacitance of the transistors and eases for the impedance matching. Two columns of shunt FETs M_1-M_2 and M_3-M_4 make the circuit balanced around this inductor. Besides, this structure also reduces the step size of varying total resistance and increases the resolution of the VCA. M_1 is stacked over M_2 and M_3 is stacked over M_4. This stacked FET structure doubles the voltage swing [12] and hence, improve the input power and linearity of the VCA. Capacitors C block the DC current and help for the impedance matching. At the gate of each transistor, large resistors (about 1 KΩ) are used to increase stability of the circuit and prevent signal leakage.

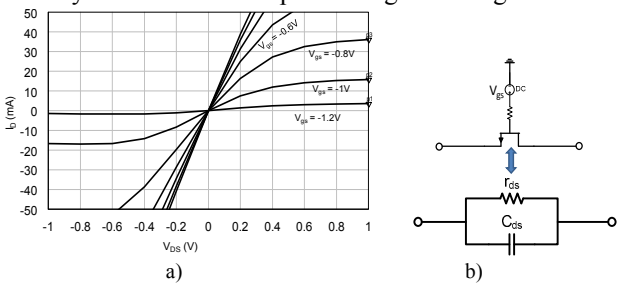

Fig. 8. a) IV-curve of a 4x75 µm transistor in triode region b) Equivalent circuit of a FET in triode region

B. VCA layout and results

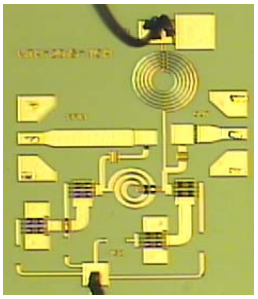

Fig. 9. Photo of test sample VCA

A test sample VCA, that has photo shown in Fig.9, is fabricated and tested. The size of this die is 0.7mm x 1mm including DC pads and RF pads. Electromagnetic simulator AXIEM of AWR is used to simulate the coupling effects and parasitic of the layout. The drain of transistor M_1 and M_3 is biased by a 1 V fixed voltage to increase the linearity. At "through" mode, the V_G is about -3 V to -5 V in order to "pinch-off" all transistors. In this case, the insertion loss caused by VCA is 2.8 dB. At "attenuation" mode, VCA controls the attenuation by changing V_G from -1.1 V to 0 V with 0.05 V step. Fig.10 shows measured attenuation of VCA for the controlled voltage V_G varying from -2 V, -1.1 V to 0 V. We can see that the VCA creates attenuation from 2.8 dB to 22 dB in this controlled voltage range. The measured return loss S_{11} and S_{22} of this VCA is shown in Fig.11a,b. According to these results, the return loss of VCA is less than -8 dB and the operating frequencies are from 6 GHz to 14 GHz.

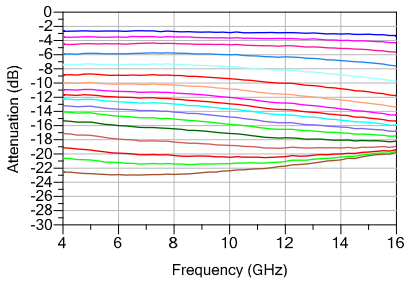

Fig. 10. Measured variable attenuation of VCA

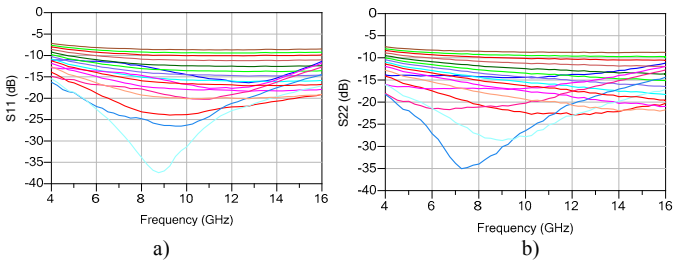

Fig. 11. Measured return loss of VCA a) S11 b) S22

IV. THE VGLNA PROTOTYPE AND MEASUREMENT RESULTS

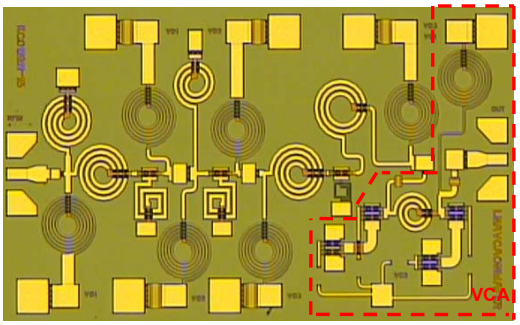

Fig. 12. The photo of VGLNA chip (LNA with integrated VCA)

The gain of the proposed LNA is controlled by integrating the proposed VCA at the output of the LNA. This LNA, therefore, has variable gain and is called variable gain LNA (VGLNA). The photo of the fabricated VGLNA chip is presented in Fig.12. The size of the whole layout is 2.2 mm x 1.2 mm. The impedance mismatch between the output of LNA and input of VCA is solved by optimizing the matching network at the interconnection. The measured S-parameters of the VGLNA is displayed in Fig.13 along with its simulated results. According to the measured results, the operation frequencies of the VGLNA are from 7.5 GHz to 10.5 GHz. In this frequency band, the VGLNA has the gain of more than 24 dB. The return loss S_{11} and S_{22} are lower than -8 dB. Fig.14 presents the variable gain of this VGLNA. When the gain control voltage varies from -1.1 V to 0 V, the gain of the VGLNA changes from 25 dB to 5 dB.

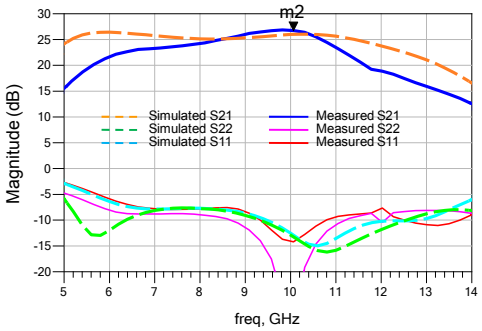

Fig. 13. Simulated and measured S-parameters of VGLNA

The measured OIP3 and Noise Figure of the proposed VGLNA are shown in Fig.15. The OIP3 is measured by feeding the two tones signal with -20 dBm power for each tone at the input. The measured results are also taken when the VGLNA is at "the highest gain" mode. The frequency separation between the two tones is 10 MHz. For the frequencies from 7.5 GHz to 10.5 GHz, the OIP3 is higher than 25 dBm. In this band, the VGLNA also achieves noise figure lower than 1.7 dB. At center frequency (9 GHz), the VGLNA achieves the minimum noise figure of 1.2 dB and the highest OIP3 of 29 dBm. The measured output P1dB of this circuit is 14 dBm at 9 GHz.

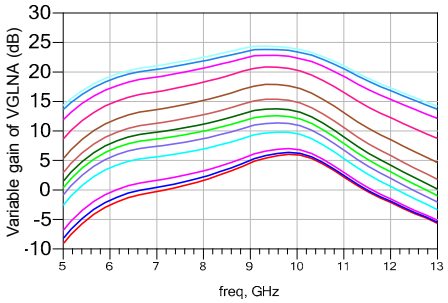

Fig. 14. Measured variable gain of VGLNA

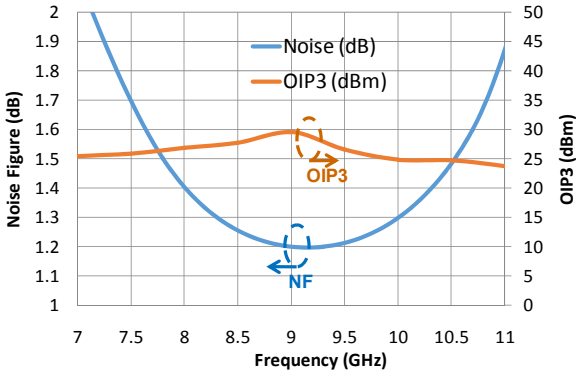

Fig. 15. Measured OIP3 and Noise Figure of VGLNA

Table 1 summaries the performance of this VGLNA and compares with the previously reported X-Band VGLNAs in the literatures. This work has high gain, wide range of gain variation, lowest noise figure and highest OIP3.

TABLE I. VGLNA PERFORMANCE SUMMARY AND COMPARISON

References	This work	[1]	[2]	[3]	[4]
Freq. (GHz)	7.5-10.5	1.3-11.9	8	8-16	9-11
Variable Gain (dB)	5 to 25	-17 to 18	12.15 to 13.63	7 to 17.5	9.5 to 16.5
NFmin (dB)	1.2	2.2	3.6	4.5	1.6
OIP3 (dBm)	29	N/A	18	15.8	18.5
Size (mm)	2.2x1.2	1.1x0.9	N/A	N/A	0.8x0.95
Process	0.15 µm pHEMT GaAs	0.25 µm SiGe BiCMOS	0.18 µm CMOS	SiGe HBT	130 nm SiGe BiCMOS

V. CONCLUSION

A highest dynamic range VGLNA for radar T/R module has been presented. This VGLNA is designed on 0.15 µm pHEMT GaAs technology and formed by a LNA integrated with a VCA. The measured results show that the proposed VGLNA has the lowest noise figure of 1.2 dB, the highest OIP3 of 29 dBm at 9 GHz. The frequency bandwidth of this

VGLNA is from 7.5 GHz to 10.5 GHz. In this band, the gain of VGLNA is higher than 24 dB and the return loss is lower than -8 dB. The output P1 dB is 14 dBm. The total size of this chip is 2.2 mm x 1.2 mm including DC pads and ground-signal-ground RF pads.

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