Verification of device model parameters for nanoscale MOSFETs

Borovik A., Kuleshov A.
Belarusian State University of Informatics and Radioelectronics,
Minsk, Belarus
borovik@bsuir.by

Tran Tuan Trung
Le Quy Don Technical University,
Hanoi, Vietnam
trttrung.mne@gmail.com

***Abstract* — A new approach to nanoscale MOSFETs electrical characteristics calculating, the essence of which is the use of adjustment factors, as well as parameter values of classic drift-diffusion models, which would effectively take into account the quantum-mechanical transport mechanisms is proposed. A modified direct search method of drift-diffusion model optimization for MOSFET with a 90 nm channel length is developed and used.**

Keywords — nanoscale MOSFET; optimization; direct search method; Darwish mobility model.

I. INTRODUCTION

Each transfer to new technological design rules leads to new physical effects appearance in MOSFETs, which is necessary to take into account by creation of new models. Standard software tools of design and simulation in microelectronics based on various models of charge carrier transport in the device structures. The physical parameters of these models are obtained as a result of experiments with specific materials, technological processes and device structures formed with certain technological design rules. It's obvious that modeling and design by using such models in other conditions with other technological design rules can lead to inadequate results. Thus, the problem of technological and device models adaptation for nanometer design rules, as well as the task of developing appropriate modeling techniques, implemented in software, are important and actual.

II. FEATURES OF THE NANOSCALE DEVICE SIMULATION

Physical models of semiconductor devices are described by the system of fundamental equations which link the electrostatic potential and charge carrier density. This system of equations is derived from Maxwell's laws and consists of Poisson equation, the continuity, transport and energy balance equations. These equations must be supplemented by the Schrodinger equation for the accurate accounting of quantum effects. The standard model of the charge carrier transport is the drift-diffusion model, which gives physically adequate results for devices manufactured in accordance with micron and submicron technological design rules. However, reducing the element size of integrated circuit leads to the appearance of new physical effects, including quantum, which should be considered during the process of models development [1, 2].

A. Decrease of mobility due to increase of the vertical electric field

Small gate dielectric thickness of the nanoscale MOSFETs leads to intensity increase of the vertical electric field $E_\perp$ under the gate up to the value when mobility decreases as a result of charge carrier scattering on surface roughness, phonons and fixed charge near surface. For small values of the intensity the dependence of the charge carrier mobility on the impurity concentration is observed, which increases with decreasing size of devices. At high transverse electric fields scattering on the surface roughness is predominant influence on the mobility in the inversion layer [2, 3].

Lombardi mobility model that describes the behavior of charge carriers in inversion layers and takes into account the carrier mobility decrease due to high degree of their scattering on the surface near the interface between the semiconductor and insulator has been used successfully for many microelectronic devices modeling. An improved version of this model where two modifications are introduced was proposed by Darwish. The first modification is related to the description of the charge carrier mobility in volume using the Klaasen model, which takes into account the Coulomb screening effect. The second modification is connected with the use of a new expression for description of the surface roughness effect [4, 5]. Contribution due surface roughness in the Darwish model is determined by the following expressions:

$$\frac{1}{\mu_{sr}} = \frac{E_\perp^{\gamma}}{\delta}, \qquad (1)$$

$$\gamma = A + \frac{\alpha_1 (n+p)}{N^{\eta}}, \qquad (2)$$

where n and p – the concentration of electrons and holes, respectively, N – the total concentration of impurities (N_D+N_A), δ – constant that depends on the details of the technology, such as oxide growth conditions (DELN.CVT for electrons in Silvaco software tools [4]), A, α_1 and η – fitting parameters (AN.CVT, ALN.CVT and ETAN.CVT respectively for electrons in Silvaco software tools).

978-1-4673-8374-5/15/$31.00 ©2015 IEEE

Contribution due acoustic phonon scattering is determined by the following expression:

$$\mu_{ac} = \frac{B}{E_{\perp}^{\ E}} + \frac{CN^{\tau}}{E_{\perp}^{\ D}}\left(\frac{300}{T_L}\right)^{\kappa}, \quad (3)$$

where T_L – the temperature of the crystal lattice, B, C, E, D, τ and κ – the empirical coefficients (BN.CVT, CN.CVT, EN.CVT, DN.CVT, TAUN.CVT and KAPPAN.CVT respectively for electrons in Silvaco software tools).

B. Decrease of longitudinal mobility

At low field intensity the carrier drift velocity depends linearly on the electric field intensity. However, from a certain value of field intensity, called the saturation intensity, charge carrier speed becomes constant and, consequently, charge carrier mobility decreases. This effect is expecially significant for transistors with short channel because reduction of channel length is faster than transistor operating voltage [2].

A method for independent determining the dependence of mobility on both the longitudinal and the transverse field for submicron transistors is described [3]. The method is based on the parameter extraction in the expression for the dependence of the carrier speed on the longitudinal E_{II} and transverse effective E_{eff} fields:

$$\mu\left(E_{\parallel}, E_{\perp}\right) = \frac{\mu_0\left(E_{\perp}\right)}{\left[1+\left(\frac{\mu_0\left(E_{\perp}\right)E_{\parallel}}{v_{sat}}\right)^{\beta}\right]^{1/\beta}}, \quad (4)$$

where μ_0 – low-field electron mobility when the effective field intensity is $E_{\perp}$; v_{sat} – saturation velocity, β – the empirical coefficient (BETAN for electrons in Silvaco software tools).

$$v_{sat} = \frac{\alpha_2}{1+\theta\exp\left(\frac{T_L}{T_{nom}}\right)}, \quad (5)$$

where α_2, θ and T_{nom} – the empirical coefficients (ALPHAN.FLD, THETAN.FLD and TNOMN.FLD respectively for electrons in Silvaco software tools).

C. The effect of depletion in the polysilicon gate

In the submicron transistor gate dielectric thickness is so small that it becomes comparable with the thickness of the depletion region in the polysilicon gate at the interface with oxide. Depletion layer increases an effective distance between gate and semiconductor, which leads to the threshold voltage increase. It is also necessary to take into account the quantum-mechanical nature of the inversion layer and introduce appropriate corrections to the classic thickness of the depletion region [2].

D. The effect of inversion layer quantization

For effective MOSFET channel control the gate oxide thickness of nanoscale structures must be several nanometers and impurity concentration in the substrate must be increased. But it reduces the thickness of the space charge region and simultaneously increases the electric field intensity at the silicon surface. Therefore the potential well for electrons becomes so narrow that the quantum-mechanical nature of the electron gas cannot be ignored [2]. The inversion layer function as a quantum well for electrons and due to the small width of the quantum well two-dimensional electron gas formes. As a result the enable energy states of the electron in the quantum well are also discrete. The consequence of this is a non-zero minimum electron energy in the potential well [3, 6].

The density of states is a parameter that determines the number of energy levels in a defined energy range. This quantity has an important physical meaning because it determines the concentration of electrons in a certain area of any material or device, as well as the intensity of electron scattering in this area. The consequence of quantum confinement is reduction of concentration of electrons at the surface and threshold voltage increase. Fig. 1 shows distribution of electrons in the MOSFET channel when using the classical and quantum mechanical approximation. Accordingly, the value of gate dielectric specific capacitance reduces and effective thickness increases [2, 3, 6].

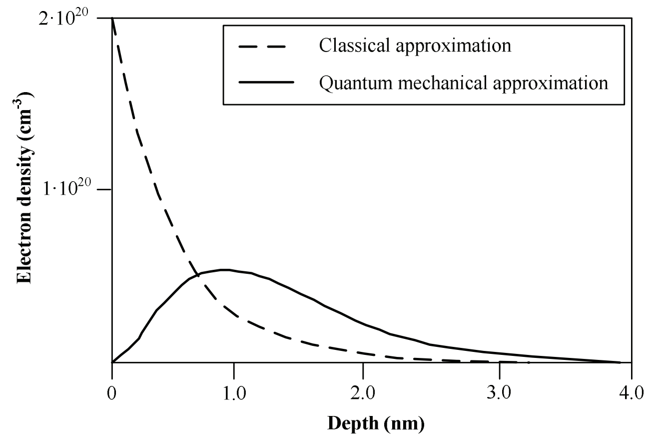


Fig. 1. Distribution of electrons in the channel.

Thus, the principal problems of nanoscale device modeling are physical effects, including quantum, occurring in the structure of new semiconductor devices, influence of which increases with decreasing geometrical dimensions of the device, as well as the complexity of simultaneously providing high accuracy of the results and acceptable simulation speed.

III. Methodologies

Generalized method for parameters verification of charge carrier transport models for MOSFETs with nanometer design rules is developed in order to adapt the parameters of the classical drift-diffusion model to obtain adequate simulation results for the electrical characteristics of nanoscale semiconductor devices (Fig. 2).

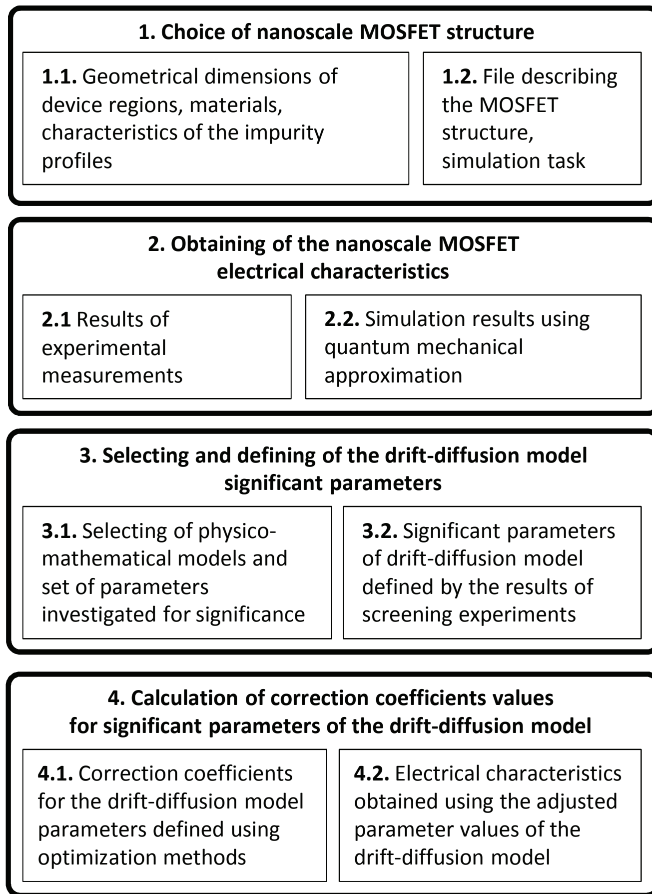


Fig. 2. Block diagram of physico-mathematical model parameter verification for MOSFETs with nanometer design rules.

The problem of identifying the most significant parameters of the transport model is solved using screening designs methodology. Screening designs are economical experimental plans that focus on determining the relative significance of many main effects. If there are more than 5 factors fractional factorial or Plackett-Burman designs are used in order to reduce the number of experiments. In comparison with fractional factor design, Plackett-Burman design is more economical with the run number a multiple of four [7].

In screening experiments, all the factors are varied between up and low levels. Those levels are chosen from desired consideration with certain values. The design of experiments describes the combination of levels in experiments. Planning conditions of Plackett-Burman design are equal numbers at up and low levels in each column, and sum of products of the elements belonging to the same experiment is equal to zero for any two columns.

After computer experiments performed results are handled to measure the effect of the factors in responses. The main effect of a factor is the difference in the response when this factor is at its up level as opposed to its low level [7, 8].

Optimization - an efficient algorithm that allows detecting the extremum region of the objective function to the specified accuracy. Methods and algorithms which allow obtaining estimates of the controlled variables vector for minimum value of the function $f(x)$ are particularly relevant. The problem of identification the function minimum is achieved by procedure of systematic obtaining a sequence of points x_0, x_1, .. x_k such that $f(x_0) > f(x_1) > ... > f(x_k) >$... After choosing the starting point it's necessary to choose the direction for the location of the next point and the step size. The mechanism of point sequence formation and its efficacy for localizing the minimum point strongly dependent on the minimized function and information that may be used to determine the next point [9].

Methods aimed at solving unconstrained optimization problem can be classified according to the type of information used in the implementation of a method, namely:

- direct search methods based on the calculation of the objective function $f(x)$ value;
- gradient methods which use values of the first derivatives of $f(x)$;
- second-order methods which use values of the first and second derivatives of $f(x)$.

In order to avoid time expenses on computing the partial derivatives if number of independent variables, five or more, a direct optimization methods are used. A common feature of these methods is the relative simplicity of the corresponding computational procedures which are easy implemented and quickly corrected.

The idea of the used optimization methods to select the reference point and evaluate the objective function values at points surrounding it. Each point corresponds to a set of parameter values. In solving the problem with two variables you can use a square model, which is a base point in the center and the test points at the vertices. Then the "best" of the five test points is selected as the next base point. Selection of the "best" point is performed by comparing standard deviation value for each of five points. If none of the node points has advantages over base point square model size can be reduced and then search should be continued. In hight dimension problems compute the objective function value is performed at all the vertices and the gravity center of the hypercube. With increasing of the problem dimension required number of objective function value calculations grows extremely fast [10].

Least square method is the oldest and the most widely used method for estimating that is used to minimize sum of squared deviations of functions from the decision variables. Least square method is usually suitable for curve fitting problem when coefficients often haven't physical meaning. Estimation can also be performed using standard deviation.

Curve relative deviation was determined as (estimated value - nominal value) / nominal value · 100%.

IV. Results

The solution of revealed problems is to optimize the drift-diffusion model in order to achieve adequate modeling of nanoscale MOS structures using experimental data or the results of more accurate modeling. To this end we will modify

the density of states in the channel region. We will also introduce correction coefficients in the expression of mobility models in the transverse and longitudinal electric field based on the analysis of the model equations and the results of screening experiments. Correction coefficients were obtained by using modified direct search method. The Darwish model is considered as mobility model in the transverse electric field. Experiments show that A, D, E, S_1, α_1, μ_{min}, μ_{max}, especially A, significantly influence the transistor threshold voltage and drain current. However, the extent of their influence depends on the size of devices [11].

For demonstration of the possibilities of the proposed drift-diffusion model adaptation approach n-channel MOSFET structure with channel length of 90 nm was used (Fig. 3) [12].

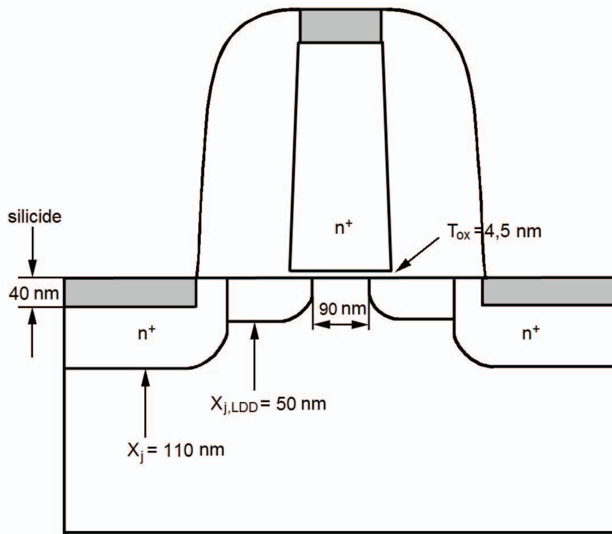


Fig. 3. N-channel MOSFET structure with channel length of 90 nm.

After the introduction of correction coefficients expression for describing contribution due acoustic phonon scattering, have the following form:

$$\mu_{ac} = \frac{B}{E_{\perp}^{0,97E}} + \frac{CN^{\tau}}{E_{\perp}^{0,97D}}\left(\frac{300}{T_L}\right)^{\kappa}. \quad (6)$$

The expression for calculating the coefficient γ:

$$\gamma = 1,0455A + \frac{\alpha_1(n+p)}{N^{\eta}}. \quad (7)$$

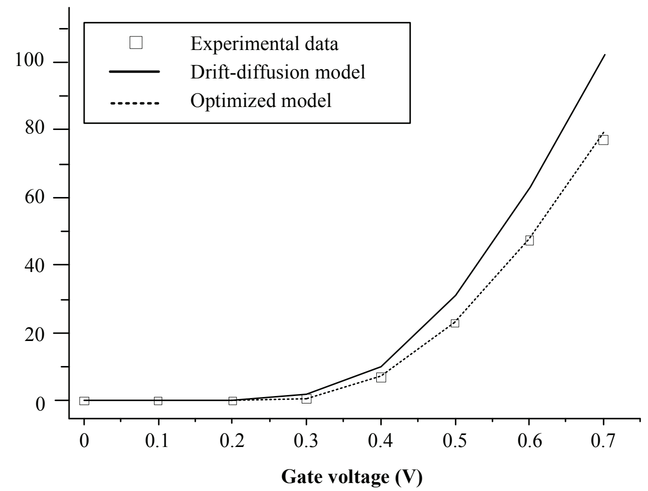
Expressions for the saturation velocity and mobility in the longitudinal electric field are of the following form:

$$v_{sat} = \frac{0,97\alpha_2}{1+\theta\exp\left(\frac{T_L}{T_{nom}}\right)}, \quad (8)$$

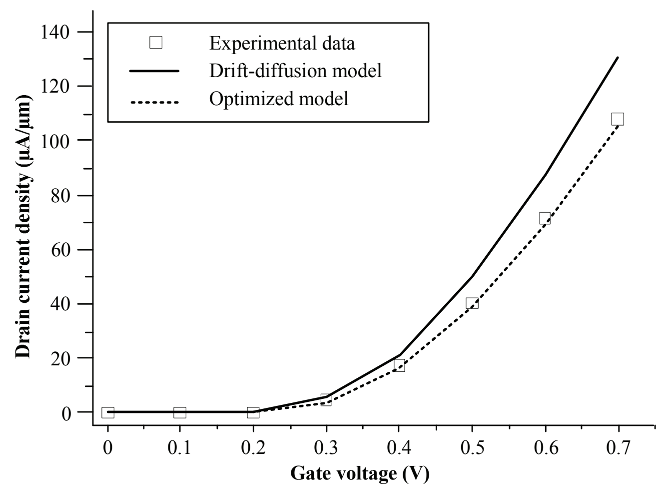
$$\mu(E_{\parallel}, E_{\perp}) = \frac{\mu_0(E_{\perp})}{\left[1+\left(\frac{\mu_0(E_{\perp})E_{\parallel}}{v_{sat}}\right)^{0,56\beta}\right]^{1/0,56\beta}}. \quad (9)$$

The new value of the effective density of states for electrons in silicon is 2.5e18 см$^{-3}$.

Fig. 4 and 5 show the MOSFET current-voltage characteristics obtained experimentally and by simulation using standard and optimized drift-diffusion model. Simulation of MOSFET is carried out by using the Darwish mobility model, Shockley-Read-Hall recombination model, Fermi-Dirac statistics. Fig. 6 shows the capacitance-voltage characteristics obtained by simulation using standard drift-diffusion model and drift-diffusion model with Bohm potential correction. In this case both the initial and optimized values of the density of states and the mobility model expressions were used. Modeling was performed using the Silvaco's software package.

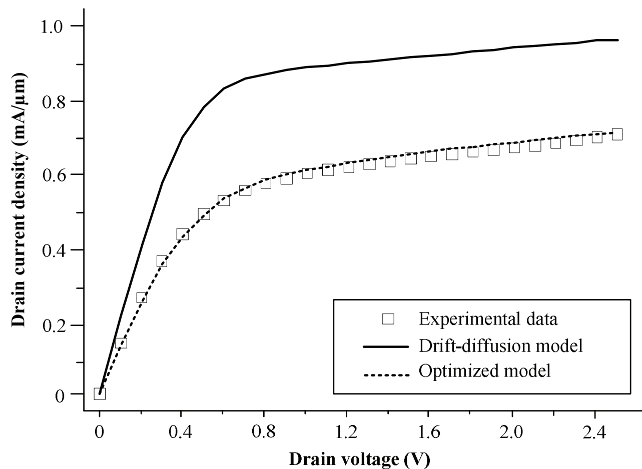


(a)

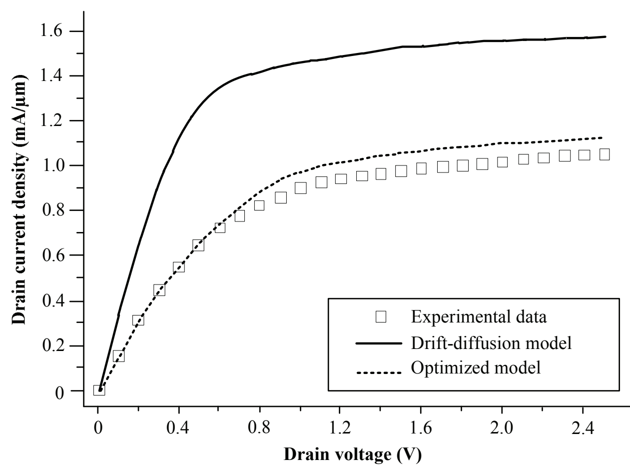


(b)

Fig. 4. Current-voltage characteristics at drain voltage 1 V (a) and 2 V (b).



(a)



(b)

Fig. 5. Current-voltage characteristics at gate voltage 2 V (a) and 3 V (b).

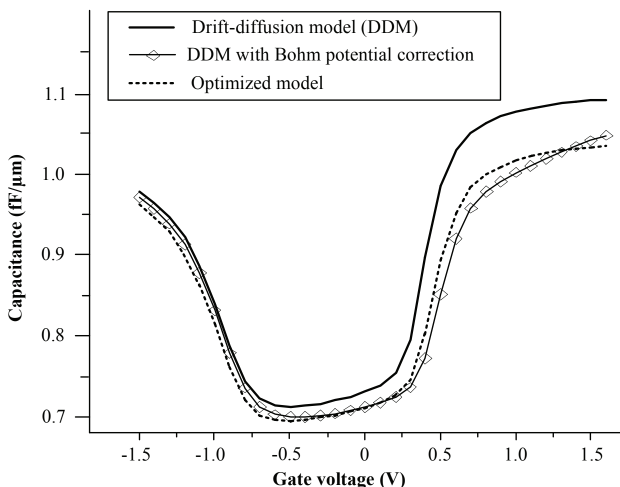


Fig. 6. Capacitance-voltage characteristics.

Obviously, the results obtained using the optimized model equations agree with the experimental data.

V. CONCLUSIONS

Results of the development and approbation methods for verification technological and device models parameters of nanoscale semiconductor devices allow us to arrive at the following conclusions:

1. The proposed method for modeling the electrical characteristics of nanoscale semiconductor devices based on the use of correction factors to the parameters of the drift-diffusion model calculated using the methods of determining the significant parameters of complex multifactor systems and optimization methods allows to obtain agreement with the experimental data with a relative error of less than 5%.

2. Correction coefficients to the drift-diffusion model parameters allow to adequately describe the electrical properties of nanoscale MOSFETs and provide reduction in calculation duration in modern software of technology and device simulation from 2 to 5 times without need for analysis of large number of significant parameters combinations.

ACKNOWLEDGMENT

This work was supported by the grant 1.1.16 of Belarusian National Scientific Research Program “Electronics and Photonics”

REFERENCES

[1] D. Vasileska, H. R. Khan, S. S. Ahmed “Quantum and Coulomb Effects in NanoDevices”, Nano-Electronic Devices, vol. 4, pp. 305-361, 2005.

[2] V. V. Denisenko MOSFET compact models for SPICE in micro- and nanoelectronics, Fizmatlit, Moscow, 2010.

[3] G.Ya. Krasnikov Structural and technological features of submicron MOSFETs, Technosphere, Moscow, 2011.

[4] ATLAS_user’s_manual.pdf, Silvaco International Incorporated, 2015. *http://www.silvaco.com/products/tcad/device_simulation/*

[5] M. N. Darwish, J. L. Lentz, M. R. Pinto, P. M. Zeitzoff, T. J. Krutsick, and H. H. Vuong, “An improved electron and hole mobility model for general purpose device simulation”, IEEE Trans. Electron Devices, vol. 44(9), pp. 1529-1538, 1997.

[6] V. Ye. Borisenko A. I. Vorobyeva, A. L. Danilyuk, E. A. Utkina., Nanoelectronics: Theory and Practice, Binom, Moscow, 2013.

[7] R. L. Plackett and J. P. Burman, "The design of optimal multifactorial experiments", Biometrika, vol. 33, pp. 305-325, 1946.

[8] J. P. C. Kleijman, “Screening designs for polyfactor experimentation”, Technometrics, vol. 17, No. 4, pp. 487-493, 1975.

[9] M. Aoki, Introduction to optimization techniques; fundamentals and applications of nonlinear programming. New York : Macmillan, 1971.

[10] G. V. Reklaitis, A. Ravindran, K. M. Ragsdell, Engineering optimization. Methods and application. A Wiley-Interscience Publication., 1983.

[11] V. Stempitsky, Trung Tran Tuan, A. Borovik “Screening design and device/technology deep-submicron MOS-FET simulation”, Proc. of Int. Workshop on New Approaches to High-Tech: Nano-Design, Technology, Computer Simulations (NDTCS’2013), pp. 85 - 87, 2013.

[12] "Well-Tempered" Bulk-Si NMOSFET Device Home Page, *http://www-mtl.mit.edu/researchgroups/Well/*.